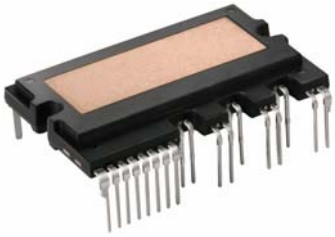
# Application Note AN-9044

## *Smart Power Module*
## *Motion-SPM in Mini DIP SPM Ver.4*
## *User's Guide*



*Written by:*

**BokKeun Song**
**JongMu Lee**
**SooHyuk Han**
**GuHo Jung**

**Motion Control System**
**HV FPG**
**FAIRCHILD SEMICONDUCTOR**

# *Contents*

# *1. Introduction*

## *1.1 Introduction*

The terms “energy-saving” and “quiet-running” are becoming very important in the world of variable speed motor drives. For low-power motor control, there are increasing demands for compactness, built-in control, and lower overall-cost. An important consideration, in justifying the use of inverters in these applications, is to optimize the total-cost-performance ratio of the overall drive system. In other words, the systems have to be less noisy, more efficient, smaller and lighter, more advanced in function and more accurate in control with a very low cost.

In order to meet these needs, Fairchild has developed a new series of compact, high-functionality, and high efficiency power semiconductor device called “Mini DIP SPM (Mini DIP Smart Power Module)”. Mini DIP SPM-based inverters are now considered an attractive alternative to conventional discrete-based inverters for low-power motor drives, specifically for appliances such as washing machines, air-conditioners, refrigerators, water pumps etc.

Mini DIP SPM combines optimized circuit protection and drive matched to the IGBT’s switching characteristics. System reliability is further enhanced by the integrated under-voltage protection function and short circuit protection function. The high speed built-in HVIC provides an opto-coupler-less IGBT gate driving capability that further reduces the overall size of the inverter system design. Additionally, the incorporated HVIC allows the use of a single-supply drive topology without negative bias.

The objective of this application note is to show the details of Mini DIP SPM power circuit design and its application to Mini DIP SPM users. This document provides design examples that should enable motor drive design engineers to create efficient optimized designs with shortened design cycles by employing Fairchild Mini DIP SPM products.

## *1.2 Mini DIP SPM Design Concept*

The key Mini DIP SPM design objective is to create a smart power module with improved reliability. This is achieved by applying existing IC and LSI transfer mold packaging technology. The Mini DIP SPM structure is relatively compact: power chips and IC chips are directly die bonded on the copper lead frame, the bare ceramic material is attached to the frame, and then molded into epoxy resin. In comparison, the conventional IPM is made of power chips bonded on a metal or ceramic substrate with the ICs and the passive components assembled on a PCB. This is then assembled into a plastic or epoxy resin case and filled up with silicon gel. The Mini DIP SPM greatly minimizes the number of parts and material types, optimizing the assembly process and overall cost.

A second important Mini DIP SPM design advantage is the realization of a product with smaller size and higher power rating. Of the low power modules released to date, the Mini DIP SPM has the highest

power density with 3A to 30A rated products built into a single package outline.

The third design advantage is design flexibility enabling use in a wide range of applications. The Mini DIP SPM series has the 3-N terminal structure with the negative rail IGBT emitters terminated separately. With this structure, shunt resistance can be placed in series with each 3-N terminal to easily sense individual inverter phase currents.

The detailed features and integrated functions of Mini DIP SPM are as follows:

- 600V/3A to 30A ratings in one package (with identical mechanical layouts)
- Low-loss efficient IGBTs and FRDs optimized for motor drive applications
- High reliability due to fully tested coordination of HVIC and IGBTs
- 3-phase IGBT Inverter Bridge including control ICs for gate drive and protection
  — High-Side Features: Control circuit under voltage (UV) protection (without fault signal output)
  — Low-Side Features: UV, Thermal Shut Down(TSD) and short-circuit (SC) protection through external shunt resistor (With fault signal output),
- Single-grounded power supply and opto-coupler-less interface due to built-in HVIC
- Active-High input signal logic resolves the startup and shutdown sequence constraint between the VCC control supply and control input providing fail-safe operation with direct connection between the Mini DIP SPM and a 3.3V CPU or DSP. Additional external sequence logic is not needed
- Divided negative DC-link terminals for inverter applications requiring individual phase current sensing
- Easy PCB layout due to built in bootstrap diode
- Isolation voltage rating of 2500Vrms for one minute
- Very low leakage current due to full molded or DBC substrate.

## *1.3 Mini DIP SPM Technology*

**POWER Devices – IGBT and FRD**

The Mini DIP SPM performance improvement is primarily the result of the technological advancement of the power devices (i.e., IGBTs and FRDs) in the 3-phase inverter circuit. The fundamental design goal is to reduce the die size and increase the current density of these power devices. The Mini DIP SPM IGBTs represent Fairchild's latest technology. Through optimized NPT IGBT design, they maintain an SOA (Safe Operating Area) suitable for motor control application while dramatically reducing the on-state conduction and turn-off switching losses. They also implement smooth switching performance without sacrificing other characteristics. The FRDs are Ultrafast diodes that have a low forward voltage drop along with soft recovery characteristics.

**Control IC – LVIC, HVIC & Bootstrap diode**

The Mini DIP SPM HVIC and LVIC driver ICs were designed to have only the minimum necessary functionality required for low power inverter drives. The HVIC has a built-in high voltage level shift function

that enables the ground referenced PWM signal to be sent directly to the Mini DIP SPM's assigned high side IGBT gate circuit. This level shift function enables opto-coupler-less interface, making it possible to design a very simple system. In addition a built-in under-voltage lockout (UVLO) protection function interrupts IGBT operation under control supply under-voltage conditions. Because the bootstrap charge-pump circuit interconnects to the low-side VCC bias internal to the Mini DIP SPM, the high-side gate drive power can be obtained from a single 15V control supply referenced to control ground. It is not necessary to have three isolated voltage sources for the high-side IGBT gate drive required in inverter systems that use conventional power modules. Mini DIP SPM V4 incorporates built in bootstrap diodes which characteristics are fast reverse recovery including bootstrap resistance characteristics, about 15 ohm.

Recent progress in the HVIC technology includes chip downsizing through the introduction of wafer fine process technology. Input control logic change from the conventional low active to high active permits direct interface to 3.3V micro-controllers or DSPs. This provides low circuit current, increased noise immunity and good performance stability against temperature variation.

**Package Technology**

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are critical in determining the Mini DIP SPM performance. A trade-off exists between heat dissipation characteristics and isolation characteristics. The key to a good package technology lies in the implementation of outstanding heat dissipation characteristics without compromising the isolation rating.

In Mini DIP SPM, a technology was developed in which bare ceramic with good heat dissipation characteristics is attached directly to the lead frame. For expansion to a targeted power rating of 20A and 30A in this same physical package size, DBC (Direct Bonding Copper) technology was applied. In addition, for optimization of cost to performance up to a power rating of 10A, full molded type technology was applied. This made it possible to achieve optimum trade-off characteristics while maintaining cost-effectiveness.

Figure 1.1 shows the cross sections of the Mini DIP SPM V4 package. In full molded packages, the lead frame structure was bent to secure the required electrical spacing. In DBC package, the lead frame and the DBC substrate are directly soldered into the Mini DIP SPM lead frame.

**Inverter System Technology**

The Mini DIP SPM package is designed to satisfy the basic UL, IEC and etc. clearance and creepage spacing safety regulations required in inverter systems. In Mini DIP SPM, 3.1mm clearance and 4mm creepage were secured in all areas where high voltage is applied. Exceptionally, 2.65mm clearance and 3.7mm creepage were secured in full molded type package. In addition, the Cu frame pattern and wire connection have been optimized with the aid of computer simulation for less parasitic inductance, which is favorable to the suppression of voltage surge at high frequency switching operation.

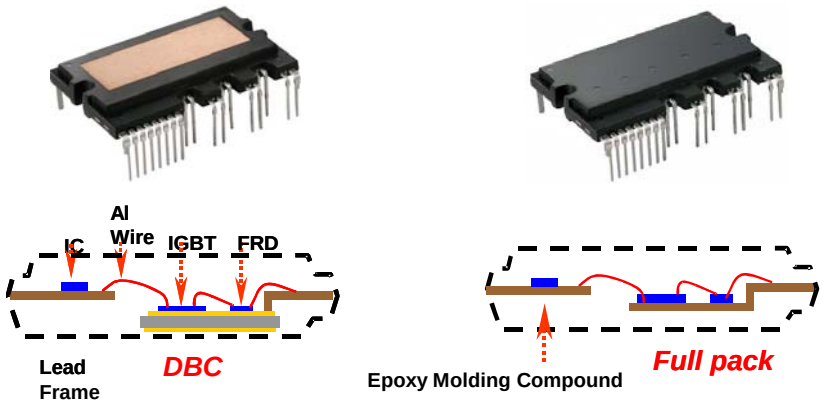



***Figure 1.1 Cross Sections of Mini DIP SPM***

HVIC is sensitive to noise since it is not a complete galvanic isolation structure but is implemented as a level shift latch logic using high voltage LDMOS that passes signals from upper side gate and lower side gate. Consequently, it was designed with sufficient immunity against such possible malfunctions as latch-on, latch-up, and latch-off caused by IGBT switching noise and system outside noise. Fairchild's Mini DIP SPM design has also taken into consideration the possibility of high side malfunction caused by short PWM pulse. Since the low voltage part and the high voltage part are configured onto the same silicon in the HVIC, it cannot operate normally when the electric potential in the high voltage part becomes lower than the ground of the low voltage part. Accordingly, sufficient margin was given to take into consideration the negative voltage level that could cause such abnormal operation. Soft turn-off function was added to secure basic IGBT SOA (Safe Operating Area) under short circuit conditions.

## *1.4 Advantage of Mini DIP SPM-driven inverter drives*

**SPM Inverter Engine Platform**

Mini DIP SPM was designed to have 3A~30A rated current of products built into a single package outline. Figure 1.2 shows the junction to case thermal resistance at each current range of the Mini DIP SPM. As seen in the figure, in the 15A, 20A and 30A range, intelligent 3-phase IGBT module with high power density (Size vs. Power) was implemented. Accordingly, in the low power range, inverter system designers are able to cover almost the entire range of 0.1KW~3KW rating in a single power circuit design using Mini DIP SPM. Since circuitry and tools can become more standardized, product development and testing process are simplified, significantly reducing development time and cost. Through control board standardization, overall manufacturing cost will be substantially reduced as users are able to simplify materials purchasing and maintain manufacturing consistency.

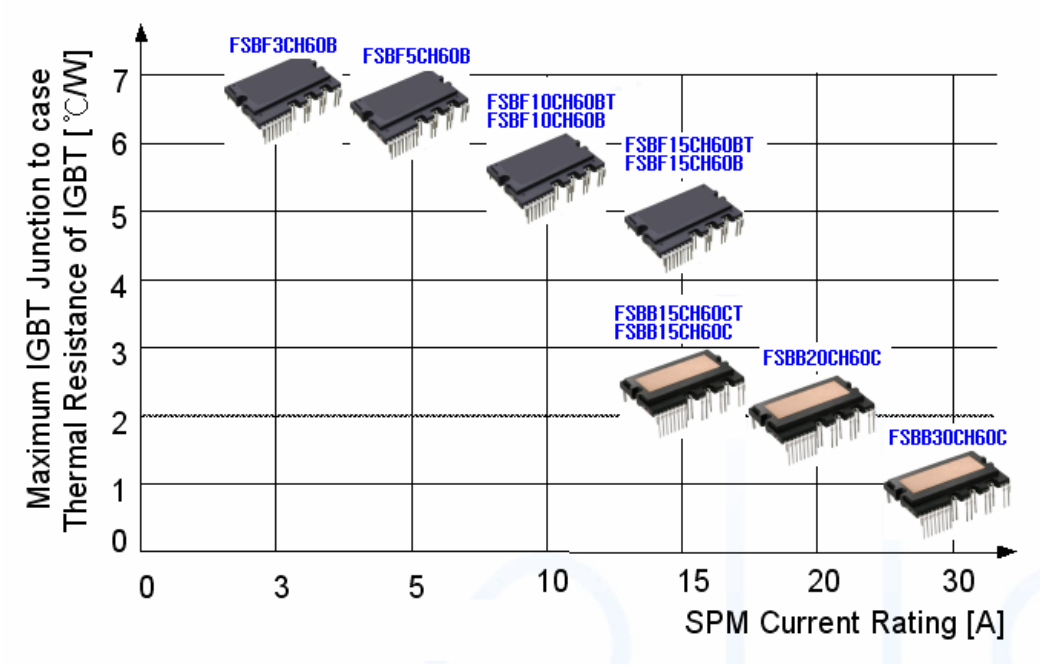



***Figure 1.2 Junction-to-case Thermal Resistance according to Current Rating of Mini DIP SPM Line-up***

**Noise Reduction**

Small package and low power loss are the primary goals of low power modules. However, in recent years, attempting to reduce power loss through excessively fast switching speed has given rise to various challenges. Excessive switching speed increases the dV/dt, di/dt, and recovery current and creates challenges such as large EMI (Electromagnetic Interference), excessive surge voltage, and high magnitude of motor leakage current. Such problems increase system cost and can even shorten motor life. Mini DIP SPM series solve these problems by adjusting the switching dV/dt to around 3kV/μsec through advanced gate drive impedance design.

Thanks to very low on-state voltage of the new generation IGBT and low forward voltage of FRD, an optimized switching speed meeting the low EMI requirement has been realized in Mini DIP SPM while keeping the total power loss at a low level equal to or less than other low power modules.

**Cost-effective Current Detection**

As sensor-less vector control and other increasingly sophisticated control methods are applied to general industrial inverters and even in consumer appliance inverters, there is a growing need to measure inverter phase current. Mini DIP SPM family has a 3-N terminal structure in which IGBT inverter bridge emitter terminal is separated. In this type of structure, inverter phase current can be easily detected simply by using external shunt resistance.

## *1.5 Summary*

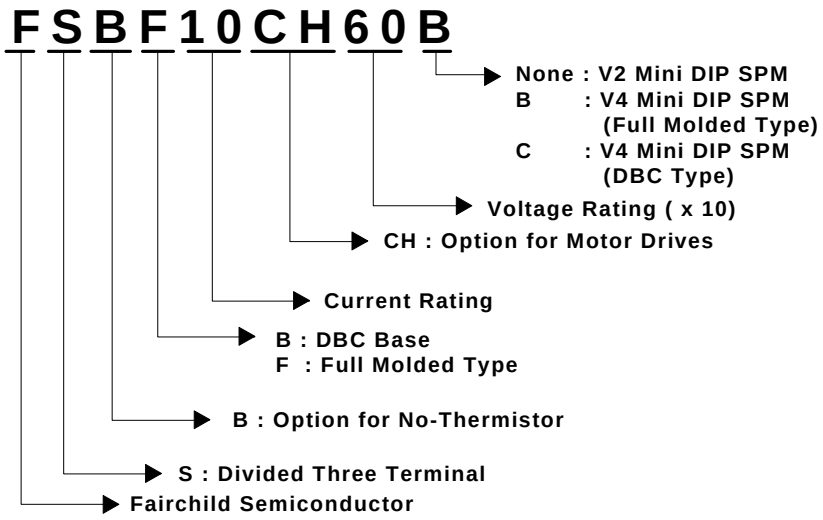
From 1999, when the SPM series was first developed, to the present, Fairchild has manufactured millions of 600V SPM series in the power range of 300W~2.2kW for consumer appliances and low power general industry applications. Today, the SPM has positioned itself as a strong inverter solution for low power motor control. With its compact size, optimized performance, high reliability, and low cost, the SPM family is accelerating the inverterization not only of low power industrial applications but also of consumer appliances. Fairchild will continue its effort to develop the next generation of SPMs optimized for a broader variety of applications and with higher power rating in mind.

For more information on Fairchild's SPM products, please visit

http://www.fairchildsemi.com/spm

# 2. Mini DIP SPM Product Outline

## 2.1 Ordering Information




## 2.2 Product Line-Up

*Table 2.1 Lineup of Mini DIP SPM Family*

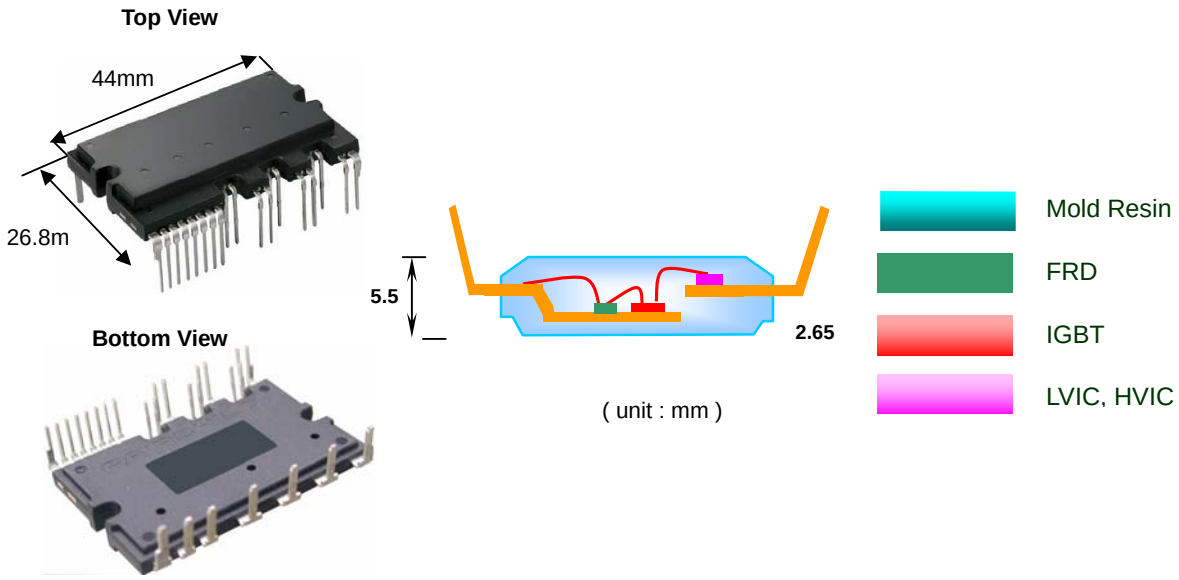
| Part Number | Rating | | Package | Isolation Voltage(Vrms) | Main Applications |
|---|---|---|---|---|---|
| | Current (A) | Voltage (V) | | | |
| FSBB30CH60C | 30 | 600 | DBC substrate (SPM27-EC) | 2500Vrms Sinusoidal, 1min | Air Conditioner Washing Machine Industrial Inverter |
| FSBB20CH60C | 20 | 600 | DBC substrate (SPM27-CC) | | |
| FSBB20CH60CT | 20 | | | | |
| FSBB15CH60C | 15 | | | | |
| FSBB15CH60CT | 15 | | | | |
| FSBF15CH60BT | 15 | 600 | Full Molded (SPM27-JA) | 2500 Vrms Sinusoidal, 1min | Air Conditioner Washing Machine Refrigerator |
| FSBF10CH60B | 10 | | | | |
| FSBF10CH60BT | 10 | | | | |
| FSBF5CH60B | 5 | | | | |
| FSBF3CH60B | 3 | | | | |

## 2.3 Applications

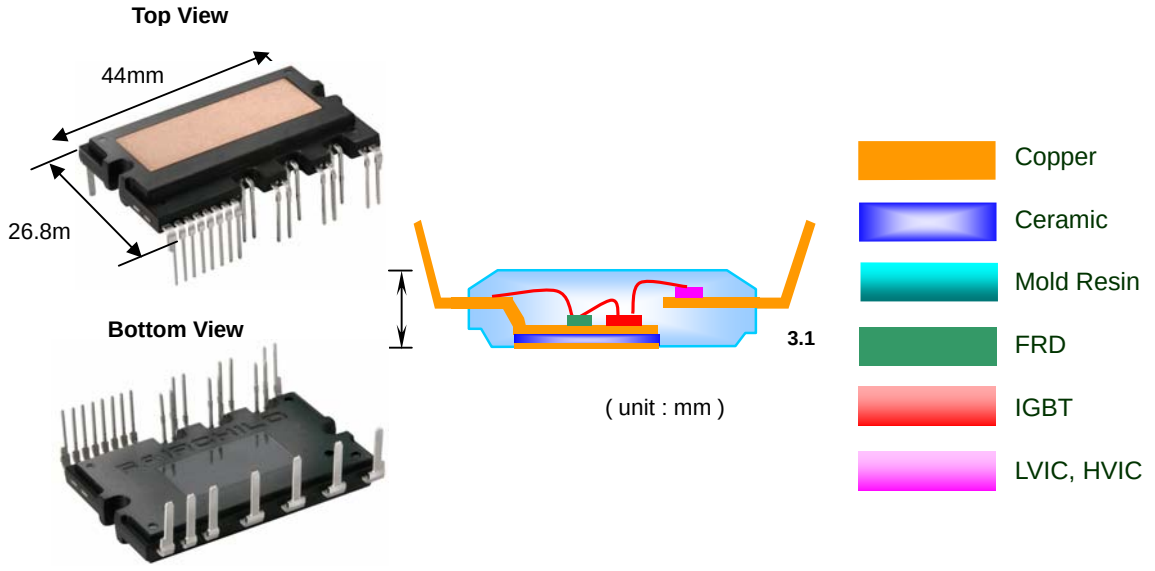
Motor drive for household electric appliances, such as air conditioners, washing machines, refrigerators, dish washers, and low power industrial applications as well.

## 2.4 Package Structure

Figure 2.1 contains a picture and an internal structure illustration of the Mini DIP SPM. The Mini DIP SPM is an ultra-compact power module, which integrates power components, high and low side gate drivers and protection circuitry for AC100 ~ 220V class low power motor drive inverter control into a dual-in-line transfer mold package.




*(a) SPM27-JA*

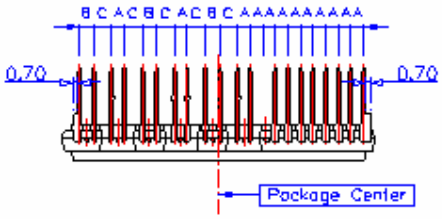



*(b) SPM27-CC, SPM27-EC*

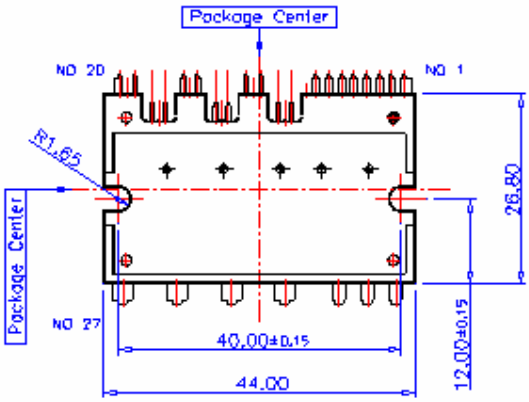
***Figure 2.2 Pictures and Package Cross section***

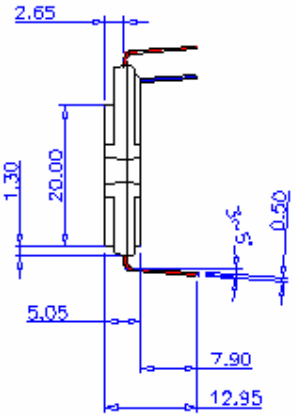
# 3. Outline and Pin Description

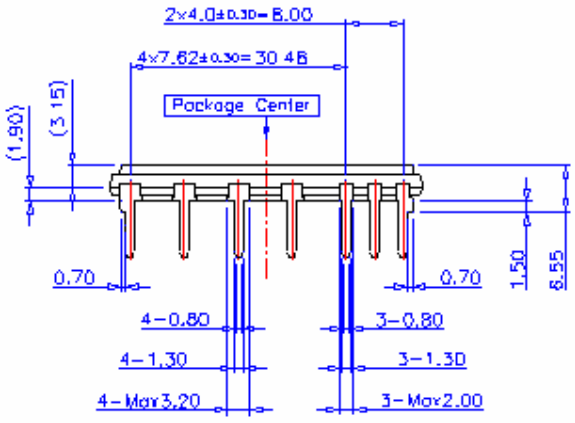
## 3.1 Outline Drawings




Lead Pitch : ±0.30
A : 1.778
B : 2.050
C : 2.531

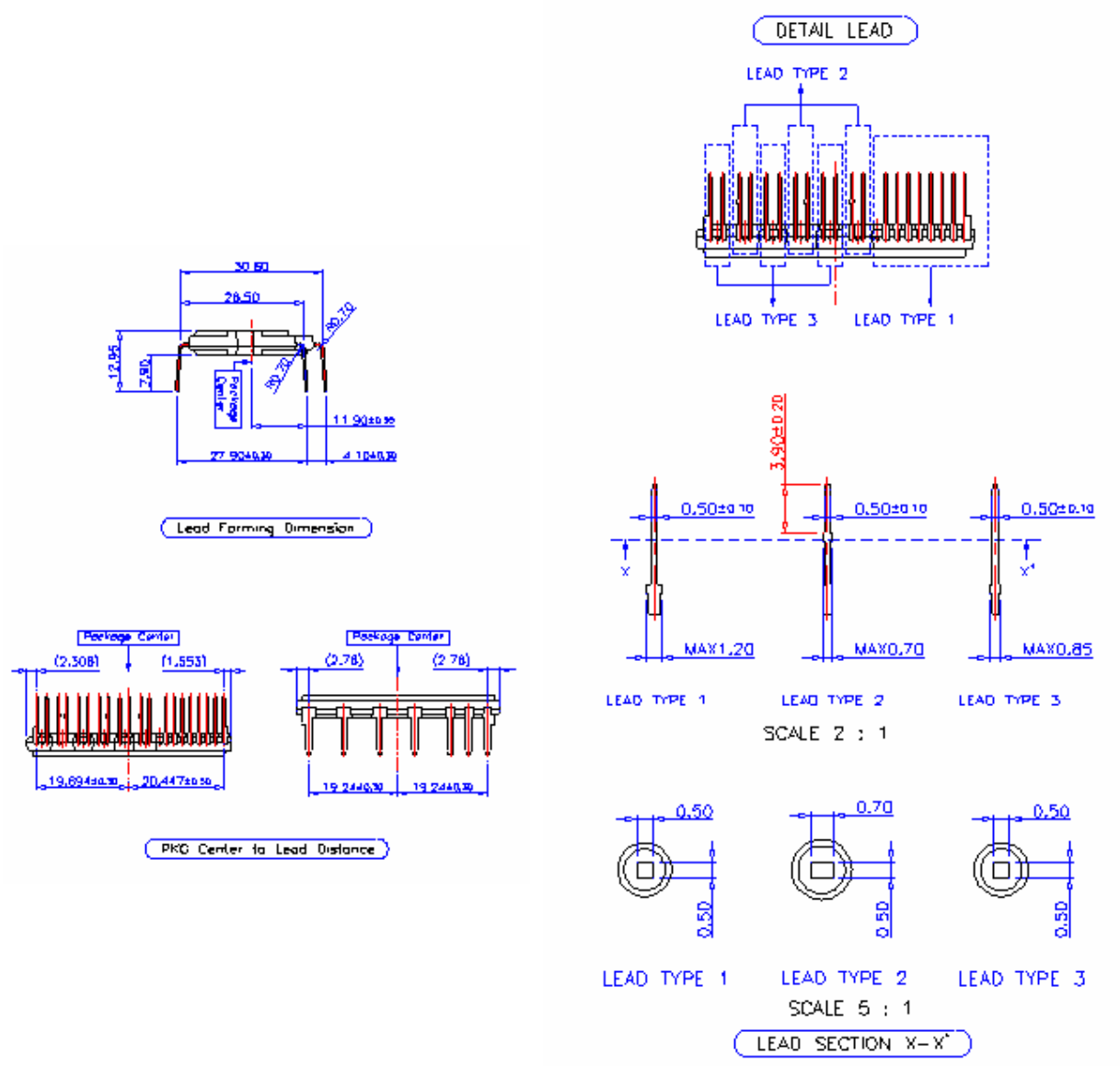


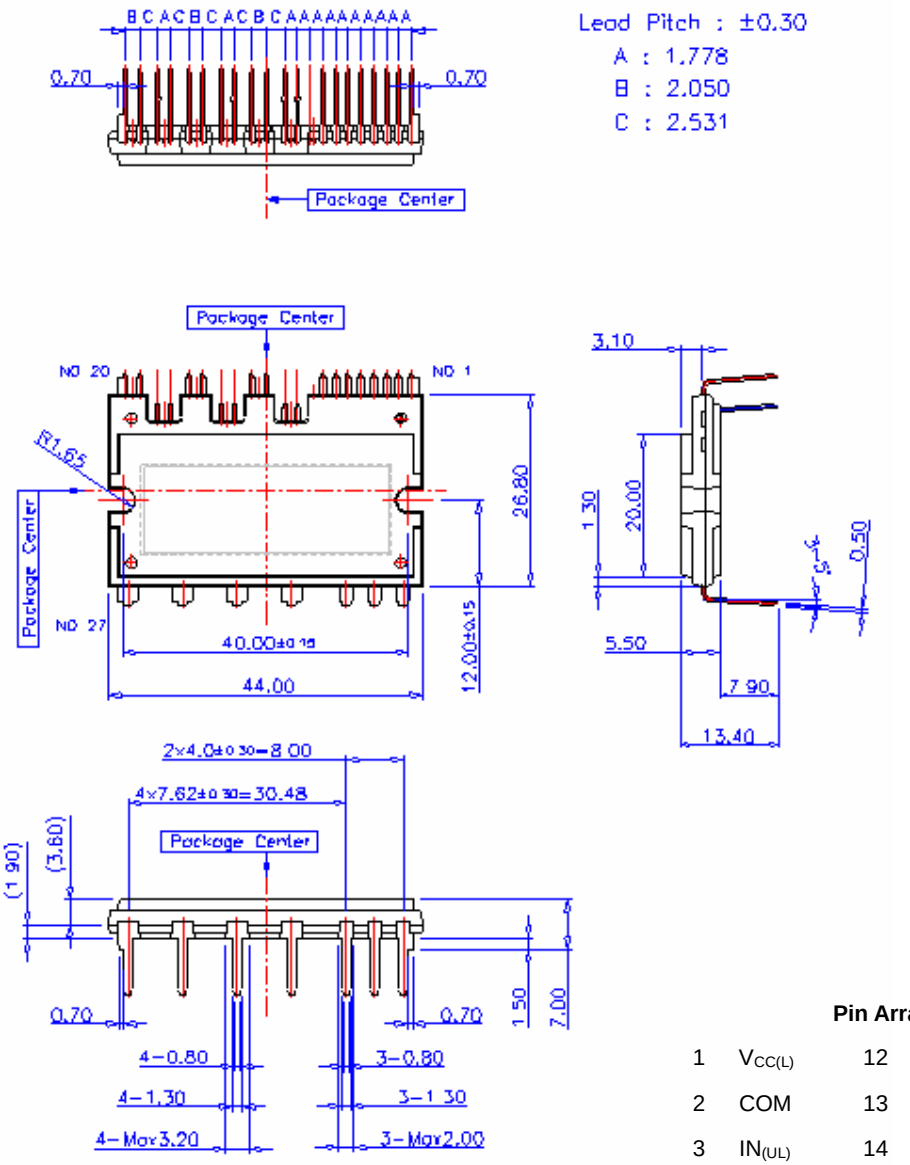




**Pin Arrangement**

| | | | | | |
|---|---|---|---|---|---|
| 1 | $V_{CC(L)}$ | 12 | $V_{S(U)}$ | 23 | $N_W$ |
| 2 | COM | 13 | $IN_{(VH)}$ | 24 | U |
| 3 | $IN_{(UL)}$ | 14 | $V_{CC(VH)}$ | 25 | V |
| 4 | $IN_{(VL)}$ | 15 | $V_{B(V)}$ | 26 | W |
| 5 | $IN_{(WL)}$ | 16 | $V_{S(V)}$ | 27 | P |
| 6 | $V_{FO}$ | 17 | $IN_{(WH)}$ | | |
| 7 | $C_{FOD}$ | 18 | $V_{CC(WH)}$ | | |
| 8 | $C_{SC}$ | 19 | $V_{B(W)}$ | | |
| 9 | $IN_{(UH)}$ | 20 | $V_{S(W)}$ | | |
| 10 | $V_{CC(UH)}$ | 21 | $N_U$ | | |
| 11 | $V_{B(U)}$ | 22 | $N_V$ | | |

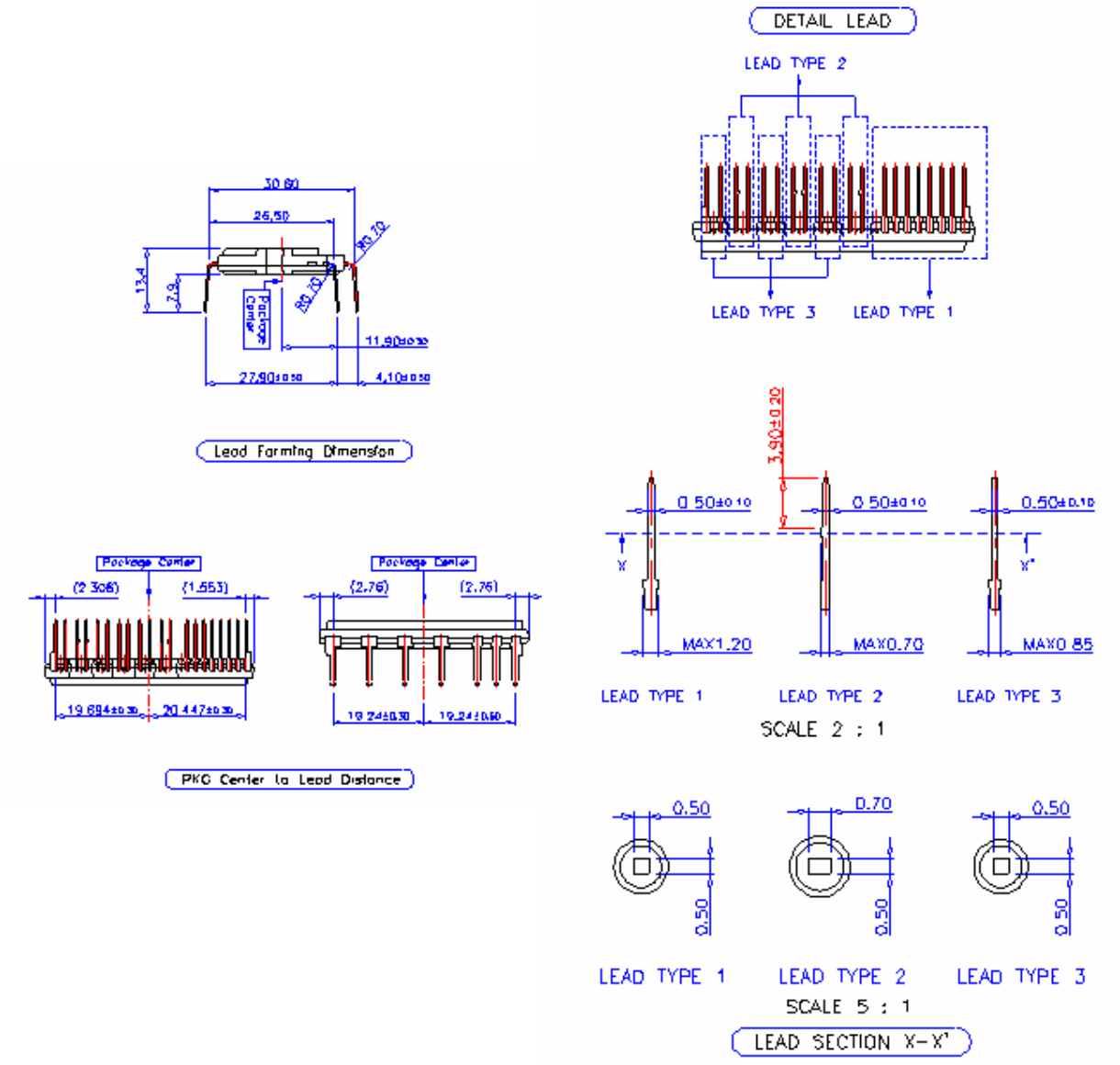

DETAIL LEAD
LEAD TYPE 2
LEAD TYPE 3
LEAD TYPE 1
30.60
28.50
12.95
7.80
11.90±0.30
27.90±0.30
4.10±0.30
Lead Forming Dimension
Package Center
(2.308)
(1.553)
19.694±0.30
20.447±0.30
Package Center
(2.78)
(2.78)
19.244±0.30
19.244±0.30
PKG Center to Lead Distance
3.90±0.20
0.50±0.10
0.50±0.10
0.50±0.10
X
X'
MAX1.20
MAX0.70
MAX0.85
LEAD TYPE 1
LEAD TYPE 2
LEAD TYPE 3
SCALE 2 : 1
0.50
0.70
0.50
0.50
0.50
0.50
LEAD TYPE 1
LEAD TYPE 2
LEAD TYPE 3
SCALE 5 : 1
LEAD SECTION X-X'

***(a) SPM27-JA***




**Pin Arrangement**

| | | | | | |
|---|---|---|---|---|---|
| 1 | $V_{CC(L)}$ | 12 | $V_{S(U)}$ | 23 | $N_W$ |
| 2 | COM | 13 | $IN_{(VH)}$ | 24 | U |
| 3 | $IN_{(UL)}$ | 14 | $V_{CC(VH)}$ | 25 | V |
| 4 | $IN_{(VL)}$ | 15 | $V_{B(V)}$ | 26 | W |
| 5 | $IN_{(WL)}$ | 16 | $V_{S(V)}$ | 27 | P |
| 6 | $V_{FO}$ | 17 | $IN_{(WH)}$ | | |
| 7 | $C_{FOD}$ | 18 | $V_{CC(WH)}$ | | |
| 8 | $C_{SC}$ | 19 | $V_{B(W)}$ | | |
| 9 | $IN_{(UH)}$ | 20 | $V_{S(W)}$ | | |
| 10 | $V_{CC(UH)}$ | 21 | $N_U$ | | |
| 11 | $V_{B(U)}$ | 22 | $N_V$ | | |




***(b) SPM27-CC, SPM27-EC***

***Figure 3.1 Package Outline Dimensions***

## *3.2 Description of the input and output pins*

Table 3.1 defines the Mini DIP SPM input and output pins. The detailed functional descriptions are as follows:

***Table 3.1 Pin descriptions***

| Pin Number | Pin Name | Pin Description |
|---|---|---|
| 1 | $V_{CC(L)}$ | Low-side Common Bias Voltage for IC and IGBTs Driving |
| 2 | COM | Low-Side Common Supply Ground |
| 3 | $IN_{(UL)}$ | Signal Input for Low-Side U Phase |
| 4 | $IN_{(VL)}$ | Signal Input for Low-Side V Phase |
| 5 | $IN_{(WL)}$ | Signal Input for Low-Side W Phase |
| 6 | $V_{FO}$ | Fault Output |
| 7 | $C_{FOD}$ | Capacitor for Fault-output Duration Time Selection |
| 8 | $C_{SC}$ | Capacitor (Low-pass Filter) for Short-Current Detection Input |
| 9 | $IN_{(UH)}$ | Signal Input for High-side U phase |
| 10 | $V_{CC(UH)}$ | High-Side Bias Voltage for U Phase IC |
| 11 | $V_{B(U)}$ | High-Side Bias Voltage for U Phase IGBT Driving |
| 12 | $V_{S(U)}$ | High-Side Bias Voltage Ground for U Phase IGBT Driving |
| 13 | $IN_{(VH)}$ | Signal Input for High-side V phase |
| 14 | $V_{CC(VH)}$ | High-Side Bias Voltage for V Phase IC |
| 15 | $V_{B(V)}$ | High-Side Bias Voltage for V Phase IGBT Driving |
| 16 | $V_{S(V)}$ | High-Side Bias Voltage Ground for V Phase IGBT Driving |
| 17 | $IN_{(WH)}$ | Signal Input for High-side W phase |
| 18 | $V_{CC(WH)}$ | High-Side Bias Voltage for W Phase IC |
| 19 | $V_{B(W)}$ | High-Side Bias Voltage for W Phase IGBT Driving |
| 20 | $V_{S(W)}$ | High-Side Bias Voltage Ground for W Phase IGBT Driving |
| 21 | $N_U$ | Negative DC-Link Input for U Phase |
| 22 | $N_V$ | Negative DC-Link Input for V Phase |
| 23 | $N_W$ | Negative DC-Link Input for W Phase |
| 24 | U | Output for U Phase |
| 25 | V | Output for V Phase |
| 26 | W | Output for W Phase |
| 27 | P | Positive DC-Link Input |

***High-Side Bias Voltage Pins for Driving the IGBT / High-Side Biase Voltage Ground Pins for Driving the IGBT***

Pins : $V_{B(U)} - V_{S(U)}$ , $V_{B(V)} - V_{S(V)}$ , $V_{B(W)} - V_{S(W)}$

- These are drive power supply pins for providing gate drive power to the High-Side IGBTs.
- The virtue of the ability to boot-strap the circuit scheme is that no external power supplies are required for the high-side IGBTs
- Each boot-strap capacitor is charged from the Vcc supply during the ON-state of the corresponding low-side IGBT.
- In order to prevent malfunctions caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins

***Low-Side Bias Voltage Pin / High-Side Bias Voltage Pins***

Pin : $V_{CC(L)}$, $V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$

- These are control supply pins for the built-in ICs.
- These four pins should be connected externally.
- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins.

***Low-Side Common Supply Ground Pin***

Pin : COM

- The Mini DIP SPM common pin connects to the control ground for the internal ICs.
- Important! To avoid noise influences the main power circuit current should not be allowed to blow through this pin.

***Signal Input Pins***

Pin : $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$

- These are pins to control the operation of the built-in IGBTs .
- They are activated by voltage input signals. The terminals are internally connected to a schmitt trigger circuit composed of 5V-class CMOS.
- The signal logic of these pins is Active-high. That is the IGBT associated with each of these pins will be turned "ON" when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the Mini DIP SPM against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Fig. 6.1.

***Short-Current Detection Pins***

Pin : $C_{SC}$

- The current sensing shunt resistor should be connected between the pin $C_{SC}$ and the low-side ground COM to detect short-current (reference Fig. 7.4)
- The shunt resistor should be selected to meet the detection levels matched for the specific application. An RC filter should be connected to the pin $C_{SC}$ to eliminate noise.
- The connection length between the shunt resistor and $C_{SC}$ pin should be minimized.

***Fault Output Pin***

Pin : $F_O$

- This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the SPM. The alarmed conditions are SC (Short Circuit) or low-side bias UV (Under Voltage) operation.
- The $V_{FO}$ output is of open collector configured. The $F_O$ signal line should be pulled up to the 5V logic power supply with approximately 4.7kΩ resistance.

***Fault Out Duration Time Selection Pin***

Pin : $C_{FOD}$

- This is the pin for selecting the fault out pulse length.
- An external capacitor should be connected between this pin and COM to set the fault out pulse length.
- The fault-out pulse width $t_{FOD}$ depends on the capacitance value of $C_{FOD}$ according to the following approximate equation : $C_{FOD} = 18.3 \times 10^{-6} \times T_{FOD}$ [F]. (18.3 is internal setting value of LVIC)

***Positive DC-Link Pin***

Pin : P

- This is the DC-link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high-side IGBTs.
- In order to suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin. (Typically Metallized Film Capacitors are used)

***Negative DC-Link Pins***

Pin : $N_U$, $N_V$, $N_W$

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side IGBT emitters of the each phase.

***Inverter Power Output Pin***

Pin : U, V, W

- Inverter output pins for connecting to the inverter load (e. g. motor).

## *3.3 Description of dummy pins*

Figure 3.2 defines the Mini DIP SPM dummy pins.

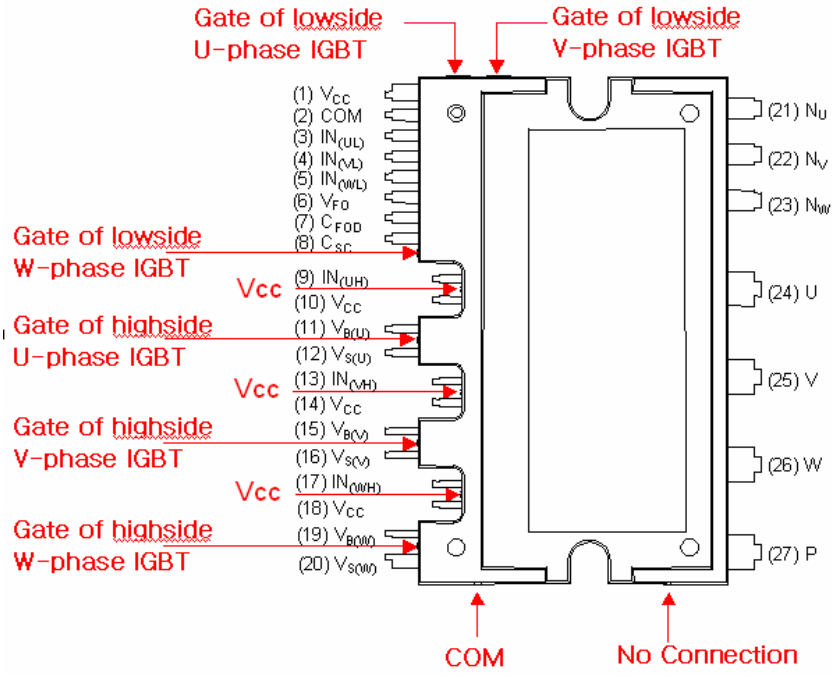



***Figure. 3.2 Description of dummy pins***

# *4. Internal Circuit and Features*

Figure 4.1 illustrates the internal block diagram of the Mini DIP SPM. It should be noted that the Mini DIP SPM consists of a three-phase IGBT inverter circuit power block and four drive ICs for control functions. The detailed features and integrated functions of Mini DIP SPM and the benefits acquired by using it are described as follows.

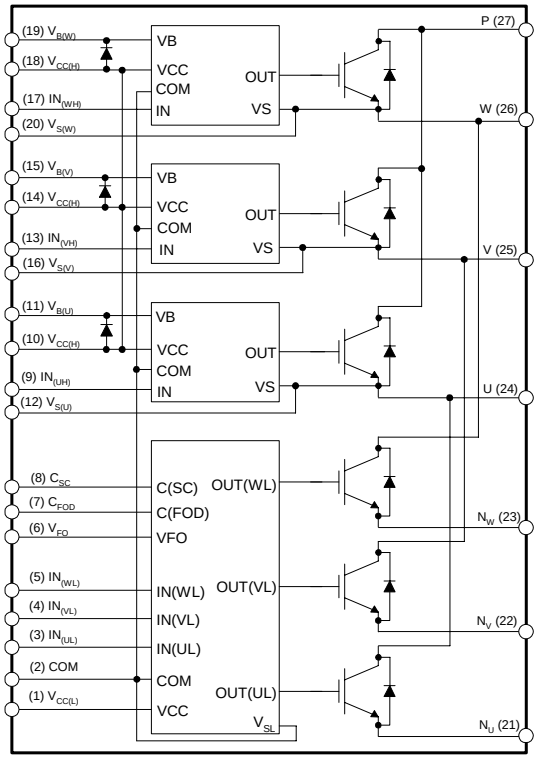



***Figure 4.1 Internal circuit***

***Features***

- 600V/3A to 30A rating in one physical package size (mechanical layouts are identical)
- Low-loss efficient IGBTs and FRDs optimized for motor drive applications
- Compact and low-cost transfer mold package allows inverter design miniaturization.
- High reliability due to fully tested coordination of HVIC and IGBTs.
- 3-phase IGBT Inverter Bridge including control ICs for gate driving and protection
  - High-side: Control circuit under voltage (UV) protection (without fault signal output)
  - Low-side: UV, Thermal Shut Down (TSD) and Short-Circuit (SC) protection by means of external shunt resistor. (with fault signal output)
- Single-grounded power supply and opto-coupler-less interface due to built-in HVIC

- IGBT switching characteristics matched to system requirement.
- Low leakage current and high isolation voltage due to DBC-based substrate
- Divided 3-N Power Terminals provide easy and cost-effective phase current sensing.
- Easy to PCB layout due to built in bootstrap diode.
- Active-high input signal logic, resolves the startup and shutdown sequence constraint between the control supply and control input, this provides fail-safe operation with direct connection between the Mini DIP SPM and a 3.3V CPU or DSP. Additional external sequence logic is not needed.

***Integrated Functions***

- Inverter high-side IGBTs: Gate drive circuit, High-voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection
- Inverter low-side IGBTs: Gate drive circuit, Short-circuit protection with soft shut-down control, Control supply circuit under-voltage protection
- Fault signaling ($V_{FO}$): Corresponding to a SC fault (low-side IGBTs) or a UV fault (low-side supply)
- Input interface: 3.3V, 5V CMOS/LSTTL compatible, Schmitt trigger input, Active high.

# *5. Absolute Maximum Ratings*

## *5.1 Electrical Maximum Ratings*

### *Turn-off Switching*

The IGBTs incorporated into the Mini DIP SPM have a 600V volt $V_{CES}$ rating. The 500V $V_{PN(Surge)}$ rating is obtained by subtracting the surge voltage (100V or less, generated by the Mini DIP SPM's internal stray inductances ) from $V_{CES}$. Moreover, the 450V $V_{PN}$ rating is obtained by subtracting the surge voltage (50V or less, generated by the stray inductance between the Mini DIP SPM and the DC-link capacitor) from $V_{PN(Surge)}$.

### *Short-circuit Operation*

In case of short-circuit turn-off, the 400V $V_{PN(PROT)}$ rating is obtained by subtracting the surge voltage (100V or less, generated by the stray inductance between the Mini DIP SPM and the DC-link capacitor) from $V_{PN(Surge)}$.

***Table 5.1 Detail description of absolute maximum ratings (FSBB15CH60C case)***

| Item | Symbol | Rating | Description |
|---|---|---|---|
| Supply Voltage | $V_{PN}$ | 450V | The maximum steady-state (non-switching mode) voltage between P-N. A brake circuit is necessary if P-N voltage exceeds this value. |
| Supply Voltage (surge) | $V_{PN(surge)}$ | 500V | The maximum surge voltage (non-switching mode) between P-N. A snubber circuit is necessary if P-N surge voltage exceeds this value. |
| Collector-emitter voltage | $V_{CES}$ | 600V | The sustained collector-emitter voltage of built-in IGBTs. |
| Each IGBT Collector current | $\pm I_C$ | 15A | The maximum allowable DC continuous IGBT collector current at Tc=25°C. |
| Junction Temperature | $T_J$ | -40 ~ 150◦C | The maximum junction temperature rating of the power chips integrated within the Mini DIP SPM is 150°C. However, to insure safe operation of the Mini DIP SPM, the average junction temperature should be limited to 125°C Although IGBT and FRD chip will not be damaged right now at $T_J$ = 150°C, its power cycles come to be decreased. |
| Self Protection Supply Voltage Limit (Short Circuit Protection Capability) | $V_{PN(PROT)}$ | 400V | Under the conditions that Vcc=13.5 ~ 16.5V, non-repetitive, less than 2μs.<br>The maximum supply voltage for safe IGBT turn off under SC “Short Circuit” or OC “Over Current” condition. The power chip may be damaged if supply voltage exceeds this specification. |

Figure 5.1 shows that the normal turn-off switching operations can be performed satisfactorily at a 450V DC-link voltage, with the surge voltage between P and N pins ($V_{PN(Surge)}$) is limited to under 500V. We can also see the difference between the hard and soft turn-off switching operation from Fig. 5.2. The hard turn-off of the IGBT causes a large overshoot (up to 100V). Hence, the DC-link capacitor supply voltage should be limited to 400V to safely protect the Mini DIP SPM. A hard turn-off, with a duration of less than approximately 2μs, may occur in the case of a short-circuit fault. For a normal short-circuit fault, the protection circuit becomes active and the IGBT is turned off very softly to prevent excessive overshoot voltage. An overshoot voltage of 30~50V occurs for this condition. Figures 5.1-5.2 are the experimental results of the safe operating area test. However, it is strongly recommended that the Mini DIP SPM should not be operated under these conditions.

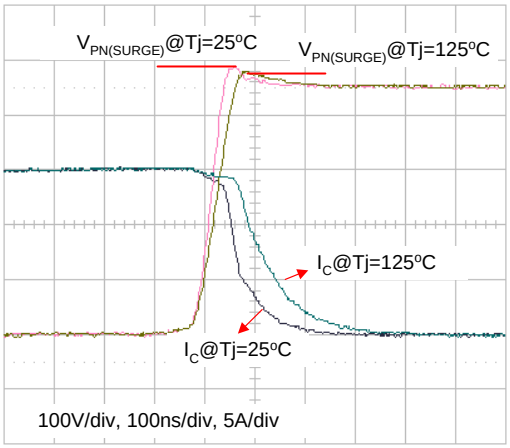



***Figure 5.1 Normal current turn-off waveforms @ $V_{PN}$=450V***

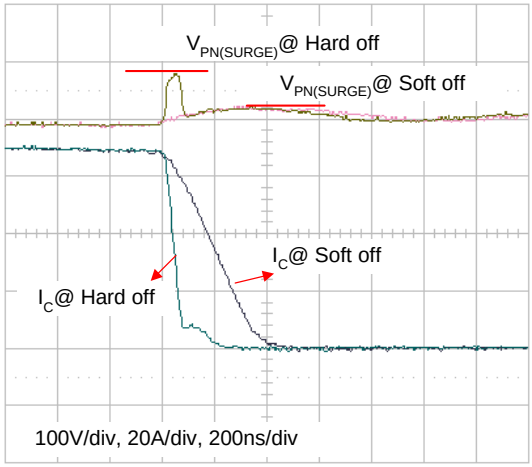



***Figure 5.2 Short-circuit current turn-off waveforms @ $V_{PN}$=400V, $T_j$ =125℃***

# 6. Interface Circuit

## 6.1 Input/Output Signal Connection

Figure 6.1 shows the I/O interface circuit between the CPU and Mini DIP SPM. Because the Mini DIP SPM input logic is active-high and there are built-in pull-down resistors, external pull-up resistors are not needed. $V_{FO}$ output is open collector configured. This signal should be pulled up to the positive side of the 5V external logic power supply by a resistor of approximate 4.7kΩ.

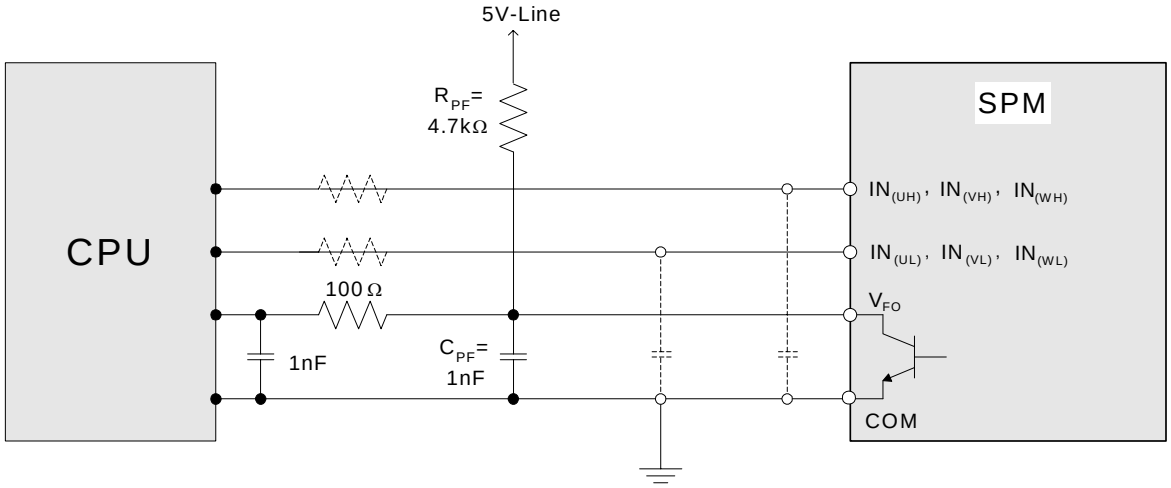



***Figure 6.1 Recommended CPU I/O Interface Circuit***

***Table 6.1 Maximum ratings of input and $F_O$ pins***

| Item | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Control Supply Voltage | $V_{CC}$ | Applied between $V_{CC(H)}$ – COM, $V_{CC(L)}$ – COM | 20 | V |
| Input Signal Voltage | $V_{IN}$ | Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ – COM $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ – COM | -0.3 ~ 17 | V |
| Fault Output Supply Voltage | $V_{FO}$ | Applied between $V_{FO}$ – COM | -0.3 ~ $V_{CC}$+0.3 | V |

The input and fault output maximum rating voltages are shown in Table 6.1. Since the fault output is open collector configured, it's rating is $V_{CC}$+0.3V, 15V supply interface is possible. However, it is recommended that the fault output be configured with the 5V logic supply, which is the same as the input signals. It is also recommended that the by-pass capacitors be placed at both the CPU and Mini DIP SPM ends of the $V_{FO}$, signal line as close as possible to each device. The RC coupling at each input (parts shown

dotted in Figure 6.1) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's PCB layout.

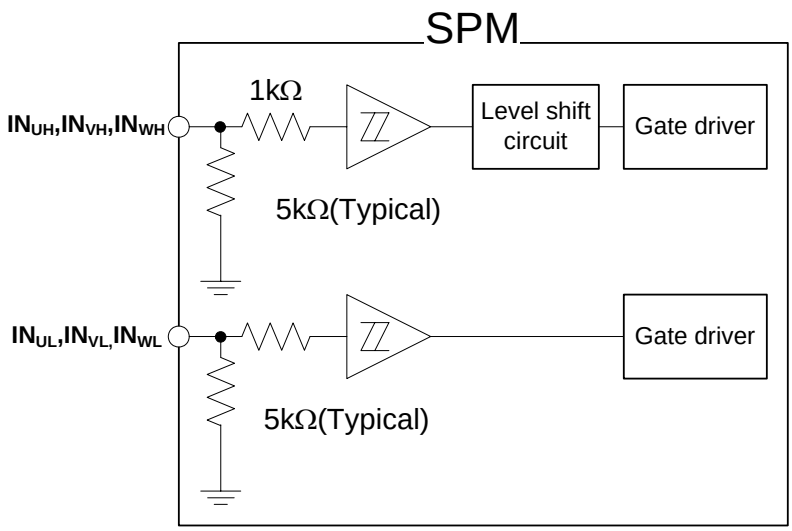



***Figure 6.2 Internal structure of signal input terminals***

The Mini DIP SPM family employs active-high input logic. This removed the sequence restriction between the control supply and the input signal during start-up or shutdown operation. Therefore it makes the system fail-safe. In addition, pull-down resistors are built in to each input circuit. Thus, external pull-down resistors are not needed reducing the required external component count. Furthermore, by lowering the turn on and turn off threshold voltage of input signal as shown in Table 6.2, a direct connection to 3.3V-class microprocessor or DSP is possible.

***Table 6.2 Input threshold voltage ratings (at Vcc = 15V, Tj = 25℃)***

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Turn on threshold voltage | $V_{IN(ON)}$ | $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(VH)}$,– COM | 2.8 | - | - | V |
| Turn off threshold voltage | $V_{IN(OFF)}$ | $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$,– COM | - | - | 0.8 | V |

As shown in Fig. 6.2, the Mini DIP SPM input signal section integrates a 5kΩ(typical) pull-down resistor. Therefore, when using an external filtering resistor between the CPU output and the Mini DIP SPM input attention should be given to the signal voltage drop at the Mini DIP SPM input terminals to satisfy the turn-on threshold voltage requirement. For instance, R = 100Ω and C=1nF for the parts shown dotted in Fig. 6.1.

## *6.2 General Interface Circuit Example*

Figure 6.3 shows a typical application circuit of interface schematic with control signals connected directly to a CPU.

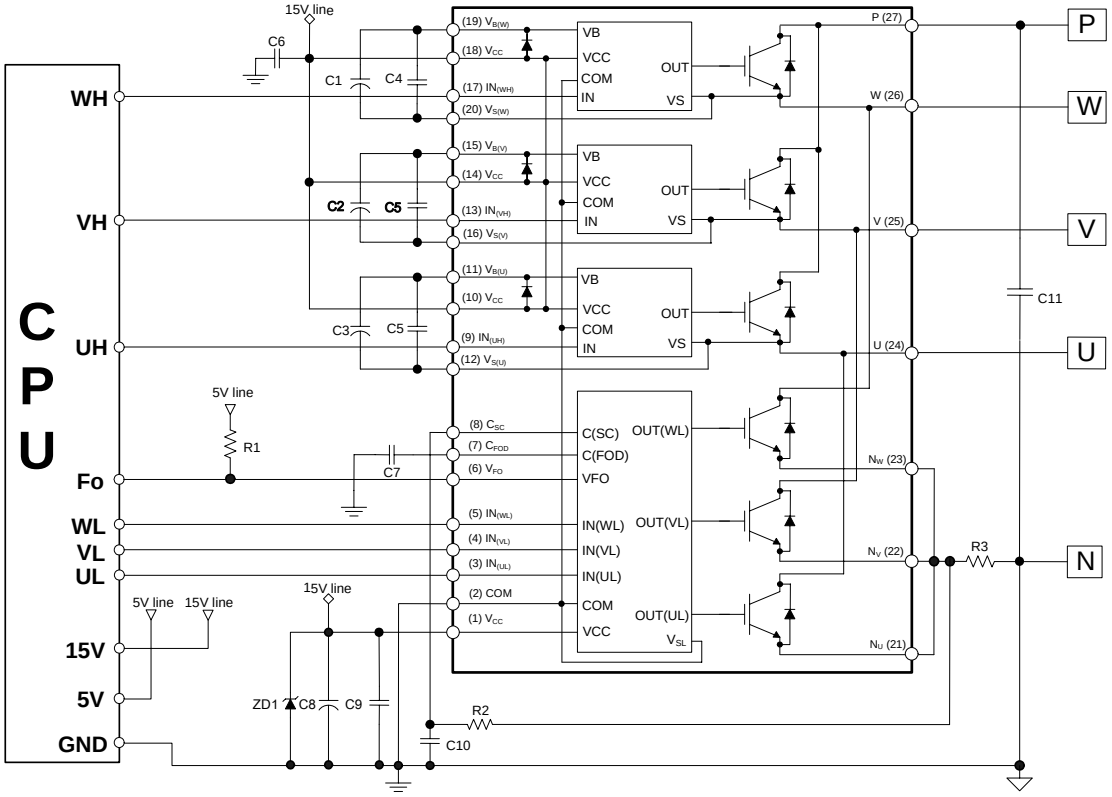



***Figure 6.3 Example of application circuit***

**Notes:**

1. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)
2. By virtue of integrating an application specific type HVIC inside the Mini DIP SPM, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
3. $V_{FO}$ output is an open collector output. This signal line should be pulled up to the positive side of the 5V logic power supply with approximately 4.7kΩ resistance. (reference Figure 6.1)
4. A $C_{SP15}$ capacitance value approximately 7 times larger than bootstrap capacitor $C_{BS}$ is recommended.
5. The $V_{FO}$ output pulse width is determined by the value of an external capacitor ($C_{FOD}$) between $C_{FOD}$ (pin7) and COM (pin2). (Example : if $C_{FOD}$ = 33 nF, then $t_{FO}$ = 1.8ms (typ.)). Please refer to the approximate equation of $C_{FOD}$ pin in page 16 for calculation method.
6. The input signals are Active-high configured. There is a internal 5kΩ pull-down resistor from each input signal line to GND. When employing RC coupling circuits between the CPU and Mini DIP SPM select the RC values such that the input signals will be compatible with the Mini DIP SPM turn-off/turn-on threshold voltages.
7. To prevent protection function errors, the $R_F$ and $C_{SC}$ wiring should be as short as possible.
8. The short-circuit protection time constant $R_FC_{SC}$ should be set in the range of 1~2μsec.

9. Each capacitor should be mounted as close to the pins of the Mini DIP SPM as possible.
10. To prevent surge destruction, the wiring between the filter capacitor and the P & Ground pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22μF between the P & Ground pins is recommended. In addition to reducing local voltage spikes, the placement and quality of this capacitor will have a direct impact on both conducted and radiated EMI.
11. Relays are used in almost all home appliances electrical equipment. These relays should be kept a sufficient distance from the CPU to prevent electromagnetic radiation from impacting the CPU.
12. Excessively large inductance due to long wiring patterns between the shunt resistor and Mini DIP SPM will cause large surge voltage that might damage the Mini DIP SPM's internal ICs. Therefore, the wiring between the shunt resistor and Mini DIP SPM should be as short as possible. Additionally, $C_{SPC15}$ (more than 1μF) should be mounted as close to the pins of the Mini DIP SPM as possible.
13. Opto-coupler can be used for electric (galvanic) isolation. When opto-couplers are used, attention should be taken to the signal logic level and opto-coupler delay time. Also, since the $V_{FO}$ output current capability is 1mA (max), it cannot drive an opto-coupler directly. A buffer circuit should be added in the primary side of the opto-coupler.

### *6.3 Recommended Wiring of Shunt Resistor and Snubber Capacitor*

External current sensing resistors are applied to detect short-circuit or phase currents. A long wiring patterns between the shunt resistors and SPM will cause excessive surges that might damage the Mini DIP SPM 's internal ICs and current detection components, and may also distort the sensing signals. To decrease the pattern inductance, the wiring between the shunt resistors and SPM should be as short as possible.

As shown in the Fig. 6.4, snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. Generally a 0.1∼0.22μF snubber is recommended. If the snubber capacitor is installed in the wrong location 'A' as shown in the Fig. 6.4, the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in the location 'B', the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current sensing signal and the SC protection level will be somewhat lower than the calculated design value. The "B" position surge suppression effect is greater than the location 'A' or 'C'. The 'C' position is a reasonable compromise with better suppression than in location 'A' without impacting the current sensing signal accuracy. For this reason, the location 'C' is generally used.

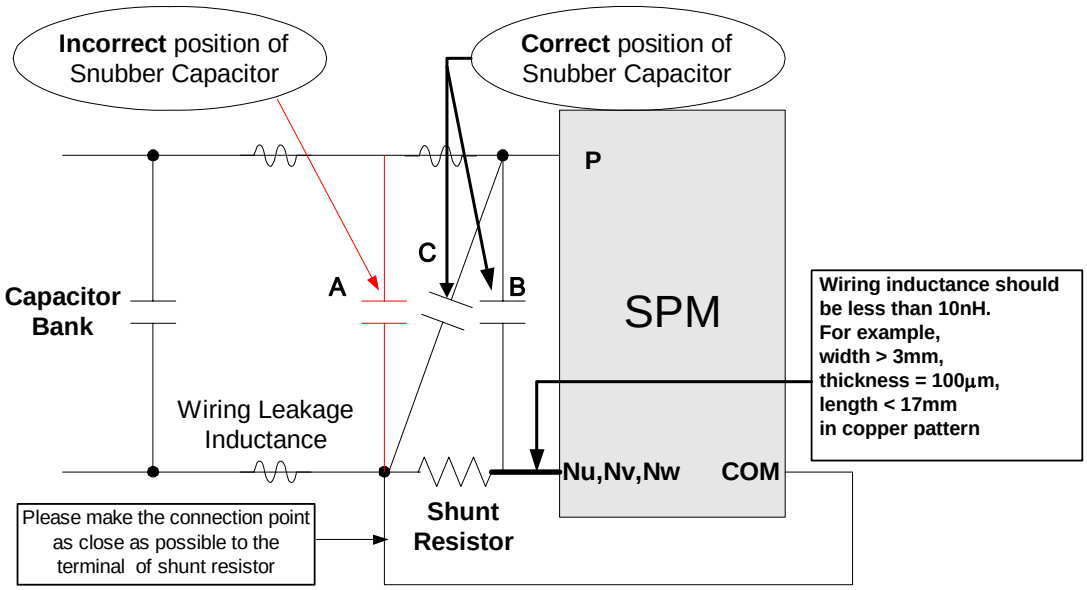



***Figure 6.4 Recommended wiring of shunt resistor and snubber capacitor***

# *7. Function and Protection Circuit*

## *7.1 SPM Functions versus Control Power Supply Voltage*

Control and gate drive power for the Mini DIP SPM is normally provided by a single 15Vdc supply that is connected to the module Vcc and COM terminals. For proper operation this voltage should be regulated to 15V ± 10% and its current supply should be larger than 60mA for SPM only. Table 7.1 describes the behavior of the SPM for various control supply voltages. The control supply should be well filtered with a low impedance electrolytic capacitor and a high frequency decoupling capacitor connected closely at the Mini DIP SPM 's pins.

High frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than ± 1V/μs. In addition, it may be necessary to connect a 24V, 0.5W zener diode across the control supply to prevent surge destruction under severe conditions.

The voltage at the module's COM terminal is different from that at the N power terminal by the drop across the sensing resistor. It is very important that all control circuits and power supplies be referred to this point and not to the N terminal. If circuits are improperly connected, the additional current flowing through the sense resistor might cause improper operation of the short-circuit protection function. In general, it is best practice to make the common reference (COM) a ground plane in the PCB layout.

The main control power supply is also connected to the bootstrap circuits that are used to establish the floating supplies for the high side gate drives.

When control supply voltage ($V_{CC}$ and $V_{BS}$) falls down under UVLO (Under Voltage Lock Out) level, IGBT will turn OFF while ignoring the input signal. To prevent noise from interrupting this function, built-in 3μsec filter is installed in both HVIC and LVIC.

Table 7.1 Mini DIP SPM Functions versus Control Power Supply Voltage

| Control Voltage Range [V] | Mini DIP SPM Function Operations |
|---|---|
| 0 ~ 4 | Control IC does not operate. Under voltage lockout and fault output do not operate. dV/dt noise on the main P-N supply might trigger the IGBTs. |
| 4 ~ 12.5 | Control IC starts to operate. As the under voltage lockout is set, control input signals are blocked and a fault signal Fo is generated. |
| 12.5 ~ 13.5 | Under voltage lockout is reset. IGBTs will be operated in accordance with the control gate input. Driving voltage is below the recommended range so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition. |
| **13.5 ~ 16.5 for $V_{CC}$**<br>**13 ~ 18.5 for $V_{BS}$** | **Normal operation. This is the recommended operating condition.** |
| 16.5 ~ 20 for $V_{CC}$<br>18.5 ~ 20 for $V_{BS}$ | IGBTs are still operated. Because driving voltage is above the recommended range, IGBTs' switching is faster. It causes increasing system noise. And peak short circuit current might be too large for proper operation of the short circuit protection. |
| Over 20 | Control circuit in the Mini DIP SPM might be damaged. |

## *7.2 Under-Voltage Protection*

The LVIC has an under voltage lockout function to protect low side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Fig. 7.1.

a1 : Control supply voltage rises :
After the voltage rises UVCCR, the circuits start to operate when next input is applied
a2 : Normal operation : IGBT ON and carrying current.
a3 : Under voltage detection ( UVCCD)
a4 : IGBT OFF in spite of control input condition
a5 : Fault output operation starts
a6 : Under voltage reset ( UVCCR)
a7 : Normal operation : IGBT ON and carrying current

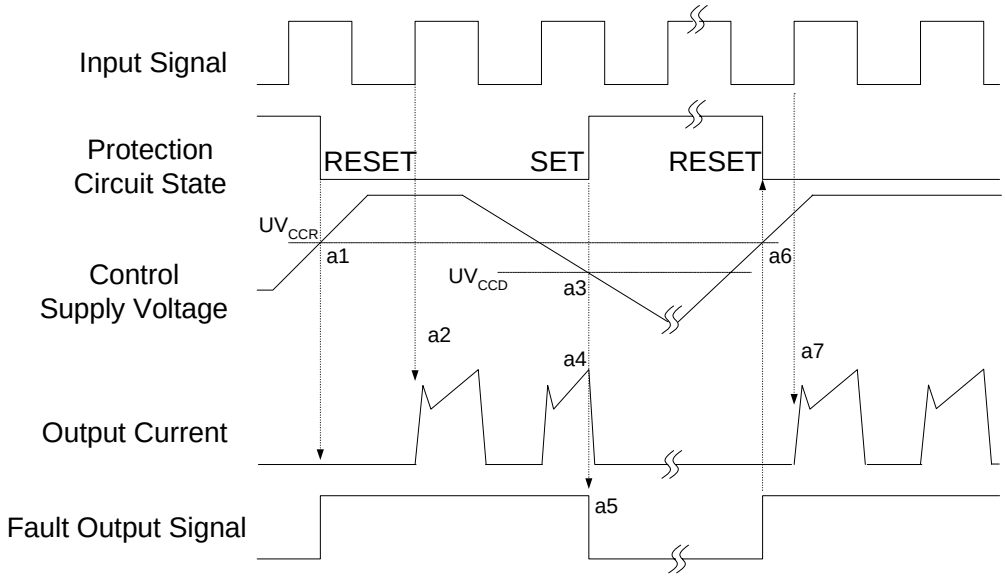



***Figure 7.1 Timing chart of low-side under-voltage protection function***

The HVIC has an under voltage lockout function to protect the high side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 7.2. A Fo alarm is not given for low HVIC bias conditions.

b1 : Control supply voltage rises: After the voltage reaches UVBSR, the circuits start to operate when next input is applied.

b2 : Normal operation: IGBT ON and carrying current.

b3 : Under voltage detection (UVBSD).

b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.

b5 : Under voltage reset (UVBSR)

b6 : Normal operation: IGBT ON and carrying current

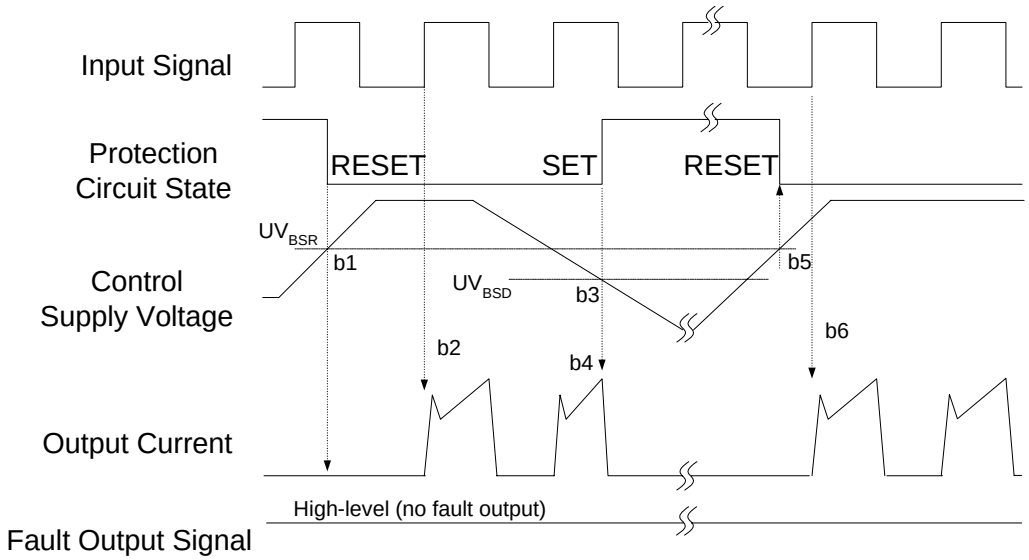



***Figure 7.2 Timing chart of high-side under-voltage protection function***

## *7.3 Short-Circuit Protection*

### *7.3.1 Timing chart of Short Circuit (SC) Protection*

The LVIC has a built-in short circuit function. This IC monitors the voltage to the $C_{SC}$ pin and if this voltage exceeds the $V_{SC(ref)}$, which is specified in the devices data sheets, then a fault signal is asserted and the lower arm IGBTs are turned off. Typically the maximum short circuit current magnitude is gate voltage dependant. A higher gate voltage results in a larger short circuit current. In order to avoid this potential problem, the maximum short circuit trip level is generally set to below 1.7times the nominal rated collector current. The LVIC short circuit protection-timing chart is shown in Figure 7.3.

(with the external shunt resistance and RC connection)

c1 : Normal operation: IGBT ON and carrying current.

c2 : Short circuit current detection (SC trigger).

c3 : Hard IGBT gate interrupt.

c4 : IGBT turns OFF softly.

c5 : Fault output timer operation starts:

The pulse width of the fault output signal is set by the external capacitor CFO.

c6 : Input “L” : IGBT OFF state.

c7 : Input “H”: IGBT ON state, but during the active period of fault output the IGBT doesn’t turn ON.

c8 : IGBT OFF state

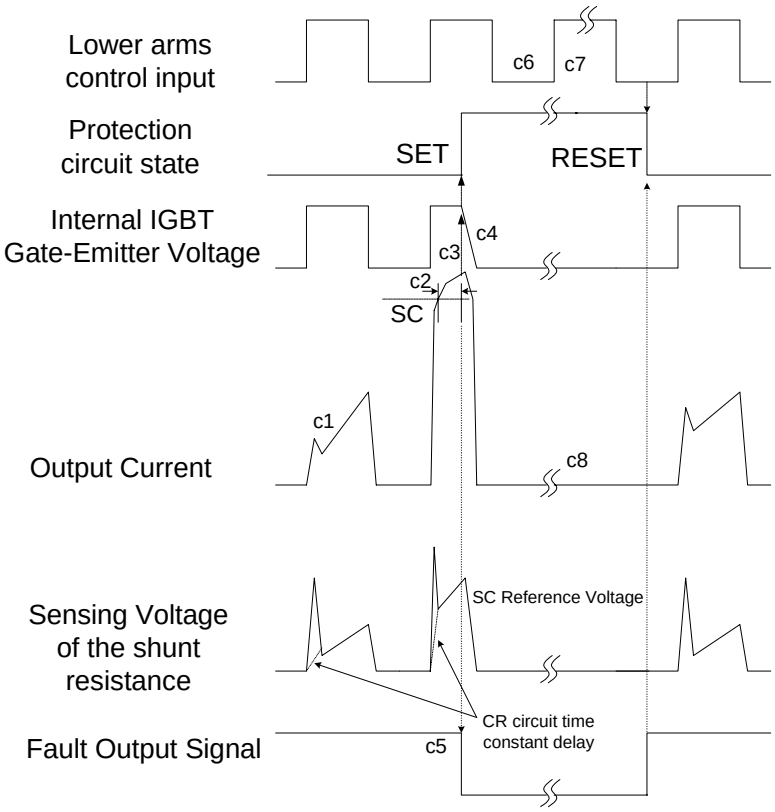



***Figure 7.3 Timing chart of short-circuit protection function***

### *7.3.2 Selecting Current Sensing Shunt Resistor*

Figure 7.4 shows an example circuit of the SC protection using 1-shunt resistor. The line current on the N side DC-link is detected and the protective operation signal is passed through the RC filter. If the current exceeds the SC reference level, all the gates of the N-side three-phase IGBTs are switched to the OFF state and the Fo fault signal is transmitted to the CPU. Since SC protection is non-repetitive, IGBT operation should be immediately halted when the Fo fault signal is given.

The internal protection circuit triggers off under SC condition by comparing the external shunt voltage to the reference SC trip voltage in the LVIC. The drive IC then interrupts low-side IGBT gates to stop IGBT operation. The value of current sensing resistor is calculated by the following expression:

$$R_{SHUNT} = \frac{V_{SC(REF)}}{I_{SC}}$$

where $V_{SC(REF)}$ is the SC reference voltage of the LVIC.

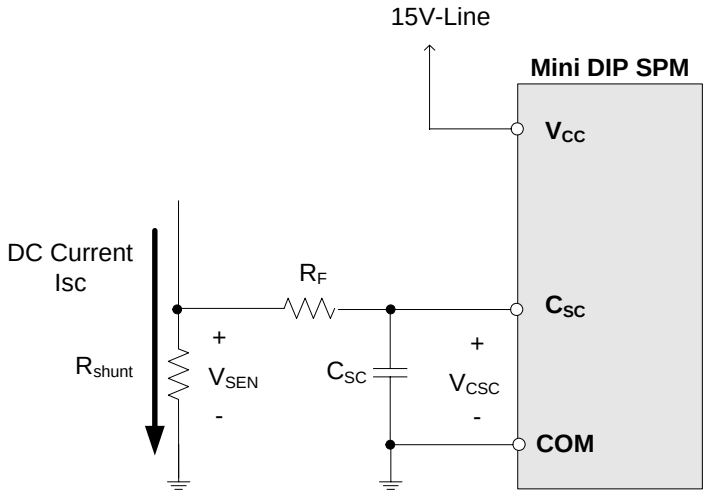



***Figure 7.4 Example of Short Circuit protection circuit with 1-shunt resistor***

An RC filter (reference $R_F$ $C_{SC}$ above) is necessary to prevent noise related SC circuit malfunction. The RC time constant is determined by the applied noise time and the IGBT withstand voltage capability. It is recommended to be set in the range of 1.5 ~ 2μs.

When the external shunt resistor voltage drop exceeds the SC protection level, this voltage is applied to the $C_{SC}$ pin via the RC filter. The filter delay time (t1) is the time required for the $C_{SC}$ pin voltage to rises to the referenced SC protection level. Table 7.2 shows the specification of the SC protection level. The IC has an internal noise elimination logic filter delay (t2) of 500nsec. The typical IC transfer time delay (t3) should be considered, too. Please, refer to the table 7.3.

***Table 7.2 Specification of SC protection reference level ' $V_{SC(REF)}$'***

| Item | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| SC trip level $V_{SC(REF)}$ | 0.45 | 0.5 | 0.55 | V |

***Table 7.3 Internal delay time of SC protection circuit***

| Item | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Internal filter delay time (t2) | - | 0.5 | 0.7 | μsec |
| IC transfer delay time (t3) | - | 0.9 | 1.3 | μsec |

Therefore the total time from the detection of the SC trip current to the gate off of the IGBT becomes:

$$T_{TOTAL} = t1 + t2 + t3$$

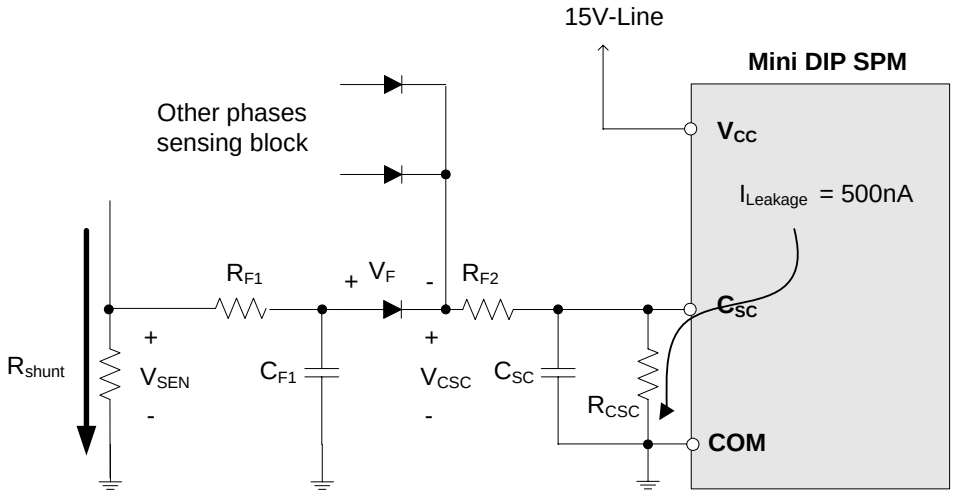



***Figure 7.5 Example of Short Circuit protection circuit with 3-shunt resistor***

The 3-shunt resistor circuit is more complicated and has more considerations than the 1-shunt resistor circuit. The 3-shunt circuit is popular since it permits detection of individual phase currents. The circuit is very cost effective, simple and provides good current sensing performance.

Figure 7.5 shows typical circuit for short-circuit detection using diodes. It should be noted that this circuit is not adequate for the precise over-current detection due to dispersion and temperature dependency of $V_F$. Also, there are additional considerations when using this circuit as follows :

1. The SC sensing signal delay time is increased. The $R_{F1}$ x $C_{F1}$ time constant delay (t4) is added so the total delay time becomes:

$$T_{TOTAL} = t1 + t2 + t3 + t4$$

2. The added diode blocks the IC leakage current (approximately 500nA) from Csc pin. If this current is applied to the capacitor Csc, the Vcsc will be increased to a somewhat higher value and causes SPM to stop gating even under normal conditions. In order to compensate for this corruption of SC current sensing voltage, Rcsc must be placed in parallel with Csc. The recommended value of Rcsc is approximately 47kΩ.
3. For the short circuit state, the diode drop voltage has to be considered to set the SC protection reference level. The equation is as illustrated below.

$$V_{SEN} = Vcsc + V_F$$

## *7.4 Fault Output Circuit*

***Table 7.4 Fault-output Maximum Ratings***

| *Item* | *Symbol* | *Condition* | *Rating* | *Unit* |
|---|---|---|---|---|
| ***Fault Output Supply Voltage*** | ***$V_{FO}$*** | ***Applied between $V_{FO}$-COM*** | ***-0.3~ $V_{CC}$+0.3*** | ***V*** |
| ***Fault Output Current*** | ***$I_{FO}$*** | ***Sink current at $V_{FO}$ pin*** | ***5*** | ***mA*** |

***Table 7.5 Electric Characteristics***

| *Item* | *Symbol* | *Condition* | *Min.* | *Typ.* | *Max.* | *Unit* |
|---|---|---|---|---|---|---|
| ***Fault Output*** | ***$V_{FOH}$*** | ***$V_{SC}$ = 0V, $V_{FO}$ Circuit: 4.7kΩ to 5V Pull-up*** | ***4.5*** | ***-*** | ***-*** | ***V*** |
| ***Supply Voltage*** | ***$V_{FOL}$*** | ***$V_{SC}$ = 1V, $V_{FO}$ Circuit: 4.7kΩ to 5V Pull-up*** | ***-*** | ***-*** | ***0.8*** | ***V*** |

Because FO terminal is an open collector type, it should be pulled up to 5V or 15V level via a pull-up resistor. The resistor has to satisfy the above specifications.

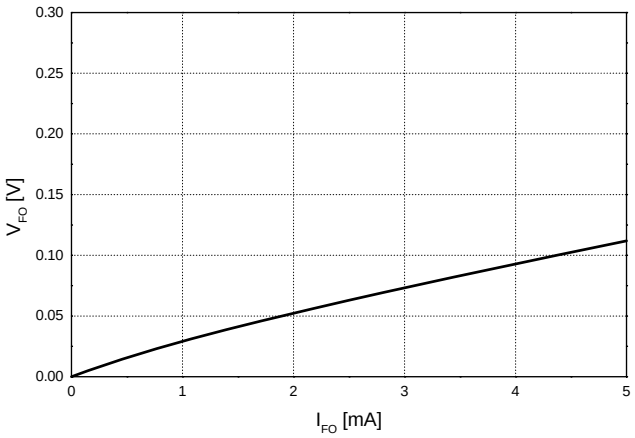



***Figure 7.6 Voltage-current characteristics of $V_{FO}$ terminal***

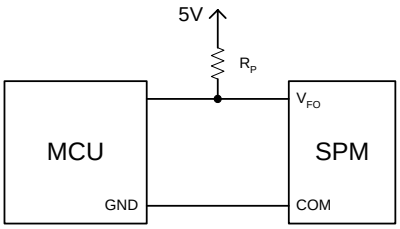



***Figure 7.7 $V_{FO}$ terminal wiring***

### *7.5 TSD (Thermal Shut-Down) Protection*

The LVIC has a built-in TSD(Thermal Shut-Down) function. This function detects LVIC temperature (not IGBT junction temperature). Purpose of this protection is to detect abnormal increase of case temperature. Cooling fan stop or loose fixing of heat sink will cause it. So this TSD function will not work effectively in the case of rapid temperature rise like motor lock condition or over current. (This protection measures LVIC temperature, so it cannot respond to rapid temperature rise of IGBT & FRD)

This TSD function detects LVIC temperature and if LVIC temperature exceeds the Td (Td : Typical 160°C), then a fault signal is asserted and the lower arm IGBTs are turned off. And then if LVIC temperature decrease under Tr (Tr : Typical 155°C), then a fault signal is released. The protection-timing chart is shown in Figure 7.8.

Td : TSD Detection

Tr : TSD Reset

ΔTdr : Hysteresis

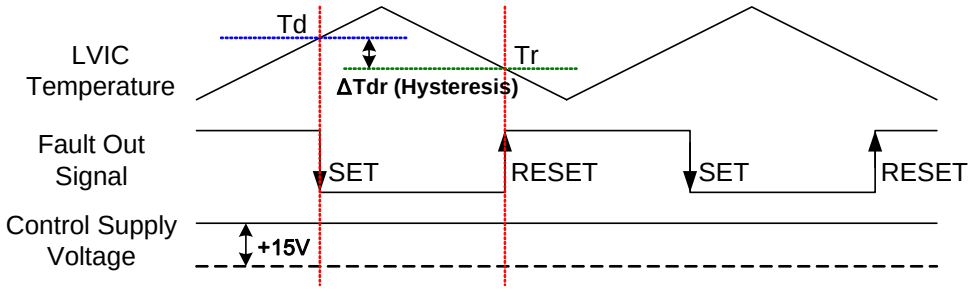



***Figure 7.8 Timing chart of LVIC TSD function***

## *8. Bootstrap Circuit*

### *8.1 Operation of Bootstrap Circuit*

The $V_{BS}$ voltage, which is the voltage difference between $V_{B\,(U,\,V,\,W)}$ and $V_{S\,(U,\,V,\,W)}$, provides the supply to the HVICs within the Mini DIP SPM. This supply must be in the range of 13.0~18.5V to ensure that the HVIC can fully drive the high-side IGBT. The Mini DIP SPM includes an under-voltage detection function for the $V_{BS}$ to ensure that the HVIC does not drive the high-side IGBT, if the $V_{BS}$ voltage drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating in a high dissipation mode.

There are a number of ways in which the $V_{BS}$ floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of an bootstrap diode, resistor and capacitor as shown in Figure 8.1. The current flow path of the bootstrap circuit is shown in Fig. 8.1. When $V_S$ is pulled down to

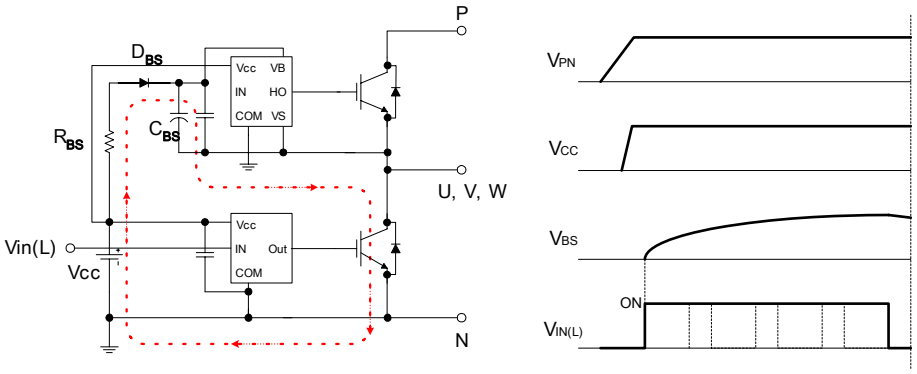
ground (either through the low-side or the load), the bootstrap capacitor ($C_{BS}$) is charged through the bootstrap diode ($D_{BS}$) and the resistor ($R_{BS}$) from the $V_{CC}$ supply.

## *8.2 Initial Charging of Bootstrap Capacitor*

An adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time ($t_{charge}$) can be calculated from the following equation:

$$t_{charge} \geq C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln\left(\frac{V_{CC}}{V_{CC} - V_{BS(\min)} - V_f - V_{LS}}\right) \qquad (8.1)$$

Vf = Forward voltage drop across the bootstrap diode
$V_{BS(min)}$ = The minimum value of the bootstrap capacitor
$V_{LS}$ = Voltage drop across the low-side IGBT or load
$\delta$ = Duty ratio of PWM




***(a) Bootstrap circuit*** ***(b) Timing chart of initial bootstrap charging***

***Figure 8.1 Bootstrap circuit operation and initial charging***

## *8.3 Selection of a Bootstrap Capacitor*

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V} \qquad (8.2)$$

Where $\Delta t$ = maximum ON pulse width of high-side IGBT
$\Delta V$ = the allowable discharge voltage of the $C_{BS.}$
$I_{leak}$= maximum discharge current of the $C_{BS}$ mainly via the following mechanisms :
Gate charge for turning the high-side IGBT on

Quiescent current to the high-side circuit in the IC
Level-shift charge required by level-shifters in the IC
Leakage current in the bootstrap diode
$C_{BS}$ capacitor leakage current (ignored for non-electrolytic capacitors)
Bootstrap diode reverse recovery charge

Practically, 1mA of $I_{leak}$ is recommended for Mini DIP SPM. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2~3 times of the calculated one. The $C_{BS}$ is only charged when the high-side IGBT is off and the $V_S$ voltage is pulled down to ground. Therefore, the on-time of the low-side IGBT must be sufficient to ensure that the charge drawn from the $C_{BS}$ capacitor can be fully replenished. Hence, inherently there is a minimum on-time of the low-side IGBT (or off-time of the high-side IGBT).

The bootstrap capacitor should always be placed as close to the pins of the SPM as possible. At least one low ESR capacitor should be used to provide good local de-coupling. For example, a separate ceramic capacitor close to the SPM is essential, if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, it should be adequate for local decoupling.

## *8.4 Built in Bootstrap Diode including around 15Ω Resistance characteristics*

From Mini DIP SPM released in Q1, 2007, built in bootstrap diode will be incorporated. When high side IGBT or diode conducts, this bootstrap diode block up the entire bus voltage. In Mini DIP SPM, the maximum rating of power supply is 450V. The actual voltage applied on the diode is 500V by adding a surge voltage of about 50V. Hence the withstand voltage of bootstrap diode is more than 600V include 100V margin. Recovery characteristics are less than max. 120ns to minimize the amount of charge that is fed back from the bootstrap capacitor into the $V_{CC}$ supply. Similarly, the high voltage reverse leakage current is important if the capacitor has to store a charge for long periods of time.

Specially, built in bootstrap diode includes around 15Ω resistance characteristics. This characteristics are used to slow down the $dV_{BS}/dt$ and it also determines the time to charge the bootstrap capacitor.

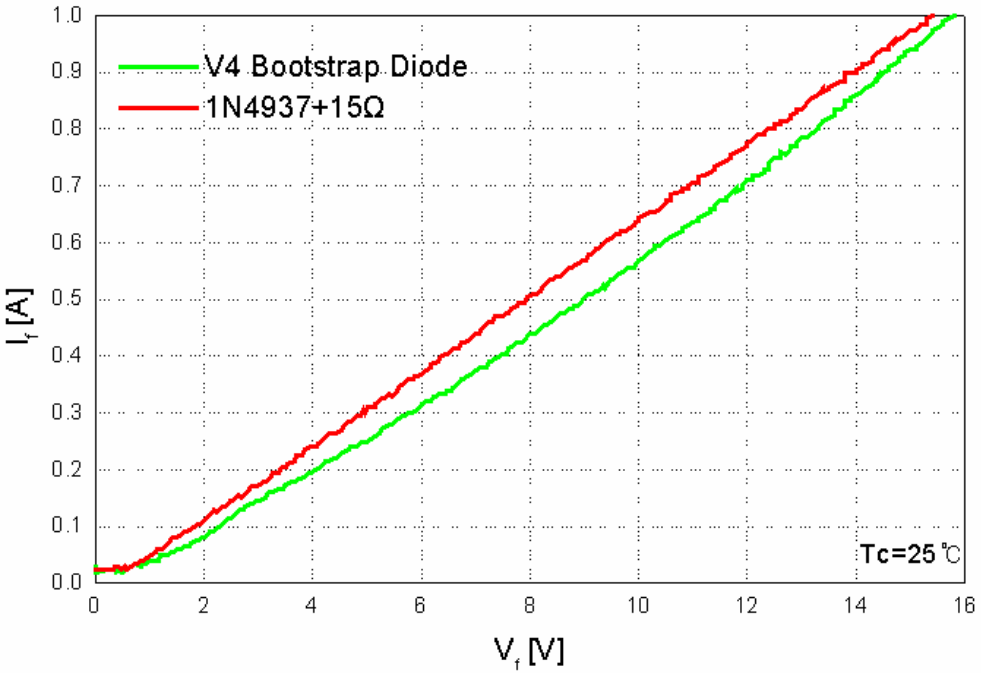



**Figure 8.2 $V_F$-$I_F$ curve of two bootstrap diode**

## *8.5 Charging and Discharging of the Bootstrap Capacitor during PWM-Inverter Operation*

The bootstrap capacitor ($C_{BS}$) charges through the built in bootstrap diode from the $V_{CC}$ supply when the high-side IGBT is off, and the $V_S$ voltage is pulled down to ground. It discharges when the high-side IGBT is on.

Example 1: Selection of the Initial Charging Time

An example of the calculation of the minimum value of the initial charging time is given with reference to equation (8.1).

Conditions:

$C_{BS}$ = 22μF

Duty Ratio of PWM(δ)= 0.5

$D_{BS}$ = built in bootstrap diode including around 15Ω resistance characteristics

$V_{CC}$ = 15V

Vf (Forward voltage drop across the bootstrap diode)= 0.5V

$V_{BS\ (min)}$ (The minimum voltage of the bootstrap capacitor)= 13V

$V_{LS}$ (Voltage drop across the low-side IGBT or load)= 0.7V

$$t_{charge} \geq 22\mu F \times 15\Omega \times \frac{1}{0.5} \times \ln(\frac{15V}{15V - 13V - 0.5V - 0.7V}) = 1.9ms$$

In order to ensure safety, it is recommended that the charging time must be at least three times longer than the calculated value.

Example 2: The Minimum Value of the Bootstrap Capacitor

Conditions:

$\Delta V$=1V

$\Delta t$=5msec

$I_{leak}$=1mA

$$C_{BS} \geq \frac{1mA \times 0.005s}{1V} = 5\mu F$$

The calculated bootstrap capacitance is 5μF. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2-3 times of the calculated one. Note that this result is only an example. It is recommended that you design a system by taking consideration of the actual control pattern and lifetime of components.

## *8.6 Recommended Boot Strap Operation Circuit and Parameters*

Figure 8.3 is the recommended bootstrap operation circuit and parameters.

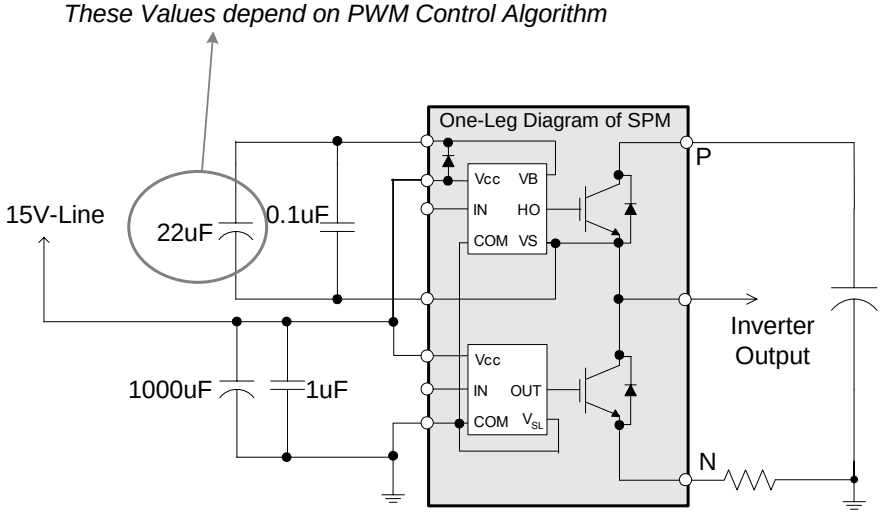



***Figure 8.3 Recommended Boot Strap Operation Circuit and Parameters***

# *9. Power Loss and Dissipation*

## *9.1 Power Loss of SPM*

The total power losses in the Mini DIP SPM are composed of conduction and switching losses in the IGBTs and FRDs. The loss during the turn-off steady state can be ignored because it is very small amount and has little effect on increasing the temperature in the device. The conduction loss depends on the dc electrical characteristics of the device i.e. saturation voltage. Therefore, it is a function of the conduction current and the device's junction temperature. On the other hand the switching loss is determined by the dynamic characteristics like turn-on/off time and over-voltage/current. Hence, in order to obtain the accurate switching loss, we should consider the DC-link voltage of the system, the applied switching frequency and the power circuit layout in addition to the current and temperature.

In this chapter, based on a PWM-inverter system for motor control applications, detailed equations are shown to calculate both losses of the Mini DIP SPM. They are for the case that 3-phase continuous sinusoidal PWM is adopted. For other cases like 3-phase discontinuous PWMs, please refer to the paper "Minimum-Loss Strategy for three-Phase PWM Rectifier, IEEE Transactions on Industrial Electronics, Vol. 46, No. 3, June, 1999 by Dae-Woong Chung and Seung-Ki Sul".

### *9.1.1 Conduction Loss*

The typical characteristics of forward drop voltage are approximated by the following linear equation for the IGBT and the diode, respectively.

$$\begin{aligned} v_I &= V_I + R_I \cdot i \\ v_D &= V_D + R_D \cdot i \end{aligned} \tag{9.1}$$

$V_I$ = Threshold voltage of IGBT $V_D$ = Threshold voltage of diode

$R_I$ = on-state slope resistance of IGBT $R_D$ = on-state slope resistance of diode

Assuming that the switching frequency is high, the output current of the PWM-inverter can be assumed to be sinusoidal. That is,

$$i = I_{peak} \cos(\theta - \phi) \tag{9.2}$$

Where $\phi$ is the phase-angle difference between output voltage and current. Using equations (9.1), the conduction loss of one IGBT and diode can be obtained as follows.

$$P_{con.I} = \frac{V_I I_{peak}}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} \xi \cos(\theta-\phi) d\theta + \frac{R_I {I_{peak}}^2}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} \xi \cos^2(\theta-\phi) d\theta \quad (9.3)$$

$$P_{con.D} = \frac{V_D I_{peak}}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} (1-\xi) \cos(\theta-\phi) d\theta + \frac{R_D {I_{peak}}^2}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} (1-\xi) \cos^2(\theta-\phi) d\theta \quad (9.4)$$

where $\xi$ is the duty cycle in the given PWM method.

$$\xi = \frac{1+MI\cos\theta}{2} \quad (9.5)$$

where MI is the PWM modulation index (MI, defined as the peak phase voltage divided by the half of dc link voltage). Finally, the integration of equation (9.3) and (9.4) gives

$$\begin{aligned} P_{con} &= P_{con.I} + P_{con.D} \quad (9.6) \\ &= \frac{I_{peak}}{2\pi}(V_I + V_D) + \frac{I_{peak}}{8}(V_I - V_D) MI\cos\phi + \frac{{I_{peak}}^2}{8}(R_I + R_D) + \frac{{I_{peak}}^2}{3\pi}(R_I - R_D) MI\cos\phi \end{aligned}$$

It should be noted that the total inverter conduction losses are six times of the $P_{con}$.

### *9.1.2 Switching Loss*

Different devices have different switching characteristics and they also vary according to the handled voltage/current and the operating temperature/frequency. However, the turn-on/off loss energy (Joule) can be experimentally measured indirectly by multiplying the current and voltage and integrating over time, under a given circumstance. Therefore the linear dependency of a switching energy loss on the switched-current is expressed during one switching period as follows.

$$Swtitching \quad energy \quad loss = (E_I + E_D) \times i \quad [joule] \quad (9.7)$$

$$E_I = E_{I.ON} + E_{I.OFF} \quad (9.8)$$

$$E_D = E_{D.ON} + E_{D.OFF} \quad (9.9)$$

where, $E_I\ i$ is the switching loss energy of the IGBT and $E_D\ i$ is for the diode. $E_I$ and $E_D$ can be

considered a constant approximately.

As mentioned in the above equation (9.2), the output current can be considered a sinusoidal waveform and the switching loss occurs every PWM period in the continuous PWM schemes. Therefore, depending on the switching frequency of $f_{SW}$, the switching loss of one device is the following equation (9.10).

$$P_{sw} = \frac{1}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}(E_I + E_D)\ i\ f_{sw}d\phi$$

$$= \frac{(E_I + E_D) f_{sw} I_{peak}}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}\cos(\theta-\phi)d\phi = \frac{(E_I + E_D) f_{sw} I_{peak}}{\pi} \quad (9.10)$$

where $E_I$ is a unique constant of IGBT related to the switching energy and different IGBT has different $E_I$ value. $E_D$ is one for diode. Those should be derived by experimental measurement. From equation (9.10), it should be noted that the switching losses are a linear function of current and directly proportional to the switching frequency.

## *9.2 Thermal Impedance*

### *9.2.1 Overview*

Semiconductor devices are very sensitive to junction temperature, i.e., as the junction temperature increases, the operating characteristics of a device are altered from normal, and the failure rate increases exponentially. This makes the thermal design of the package a very important factor in the device development stage, and also in an application field.

To gain insight into the device's thermal performance, it is normal to introduce thermal resistance, which is defined as the difference in temperature between two closed isothermal surfaces divided by the total heat flow between them. For semiconductor devices, two temperatures are junction temperature, $T_j$ and reference temperature, $T_x$, and the amount of heat flow is equal to the power dissipation of a device during operation. The selection of a reference point is arbitrary, but usually the hottest spot on the back of a device on which a heat sink is attached is chosen. This is called junction-to-case thermal resistance, $R_{\theta jc}$. When the reference point is an ambient temperature, this is called junction-to-ambient thermal resistance, $R_{\theta ja}$. Both the thermal resistances are used for the characterization of a device's thermal performance. $R_{\theta jc}$ is usually used for heat sink carrying devices while $R_{\theta ja}$ is used in other cases. Figure 9.1 shows a thermal network of heat flow from junction-to-ambient for the SPM including a heat sink. The dotted component of $R_{\theta ca}$ can be ignored due to its large value.

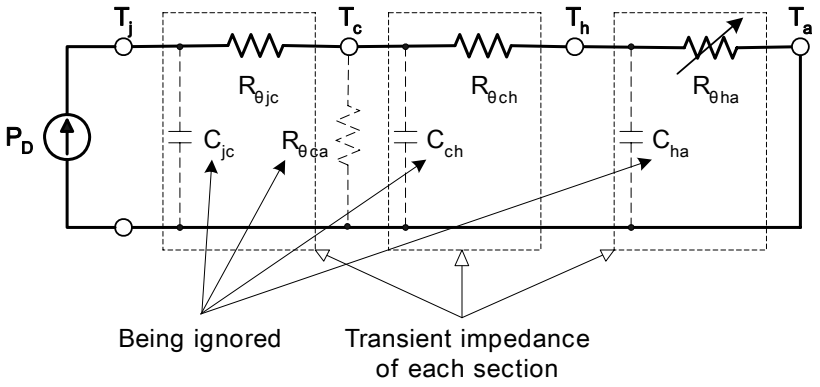



***Figure 9.1 Transient thermal equivalent circuit with a heatsink.***

The thermal resistance of the SPM is defined in the following equation,

$$R_{\theta jc} = \frac{T_j - T_c}{P_D} \tag{9.11}$$

where $R_{\theta jc}$ ($^oC/W$) is the junction-to-case thermal resistance, and $P_D$(W), $T_j$ ($^oC$) and $T_c$ ($^oC$) are power dissipation per device, junction temperature and case reference temperature, respectively. By replacing $T_c$ with $T_a$ (ambient temperature), the junction-to-ambient thermal resistance $R_{\theta ja}$ can be obtained as following,

$$R_{\theta ja} = \frac{T_j - T_a}{P_D} \tag{9.12}$$

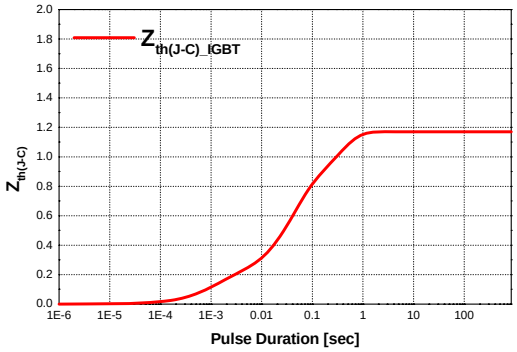
where $R_{\theta ja}$ indicates the total thermal performance of the SPM including the heat sink. Basically $R_{\theta ja}$ is a serial summation of various thermal resistances, $R_{\theta jc}$, $R_{\theta ch}$ and $R_{\theta ha}$.

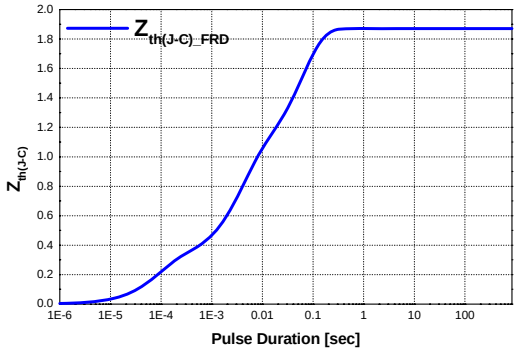
$$R_{\theta ja} = R_{\theta jc} + R_{\theta ch} + R_{\theta ha} \tag{9.13}$$

where $R_{\theta ch}$ is contact thermal resistance due to the thermal grease between the package and the heat sink, and $R_{\theta ha}$ is heat sink thermal resistance, respectively. From the equation (9.13), it is clear that minimizing $R_{\theta ch}$ and $R_{\theta ha}$ is an essential application factor to maximize the power carrying ability of the SPM as well as the minimizing of $R_{\theta jc}$ itself. An infinite heat sink will result if $R_{\theta ch}$ and $R_{\theta ha}$ are reduced to zero and the case temperature $T_c$ is locked at the fixed ambient temperature $T_a$. Usually, the value of $R_{\theta ch}$ is proportional to the thermal grease thickness and governed by the skill at the assembly site, while $R_{\theta ha}$ can be handled to some extent by selecting an appropriate heat sink.

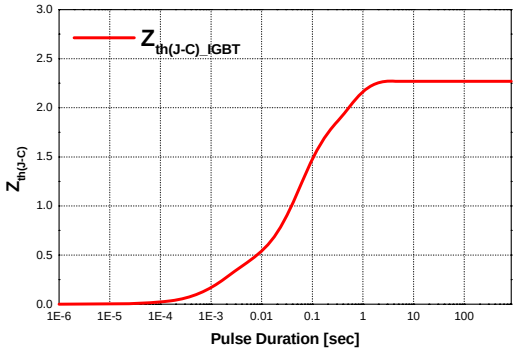
In practical operation, the power loss $P_D$ is cyclic and therfore the transient RC equivalent circuit shown in Fig. 9.1 should be considered. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature, and thus permits a heavier loading of the SPM. Figure 9.2 shows the normalized thermal impedance curves of FSBB30CH60C, FSBB15CH60C, FSBF10CH60B and FSBF3CH60B. The

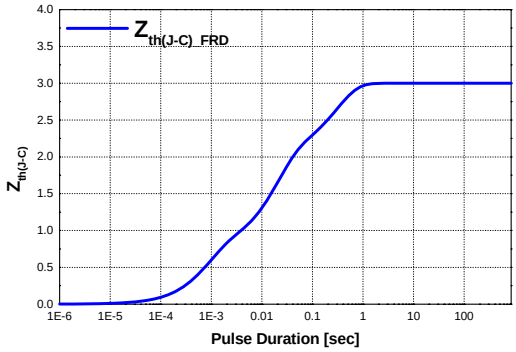
thermal resistance goes into saturation in about 10 seconds. Other kinds of SPM also show similar characteristics.



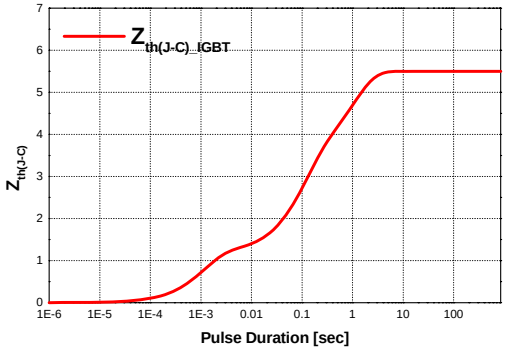



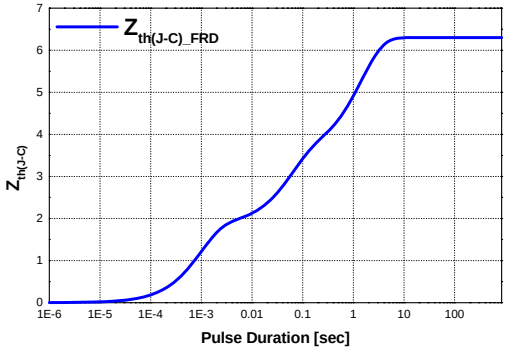

**(a) FSBB30CH60C**



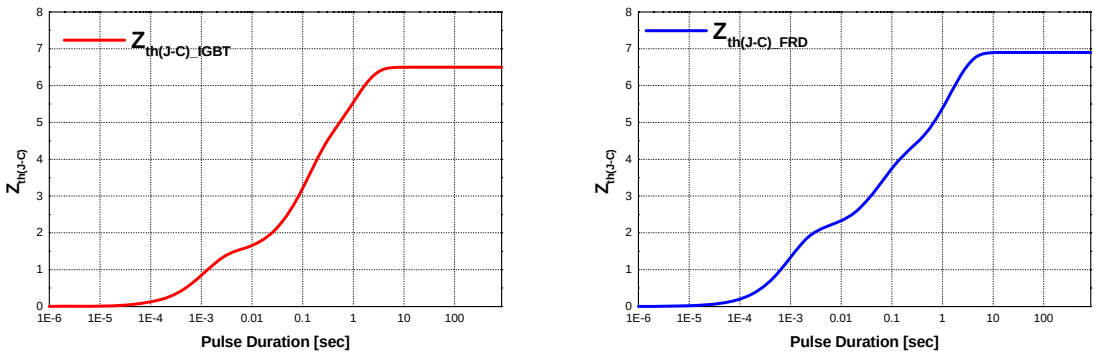




**(b) FSBB15CH60C**




**(c) FSBF10CH60B**




**(d) FSBF3CH60B**

***Figure 9.2 Normalized Thermal impedance curves.***

### *9.2.2 Measurement Method*

During the thermal resistance test, $T_j$, $T_c$ (or $T_a$) and $P_D$ should be measured. Since $T_c$, $T_a$ and $P_D$ can be measured directly, the only unknown constant is the junction temperature, $T_j$. The Electrical Test Method (ETM) is widely used to measure the junction temperature. The ETM is a test method using the relationship between forward drop voltage and junction temperature. This relationship is an intrinsic electro-thermal property of semiconductor junctions, and is characterized by a nearly linear relationship between the forward-biased drop voltage and the junction temperature, when a constant forward-biased current (sense current) is applied. This voltage drop of the junction is called Temperature Sensitive Parameter (TSP). Figure 9.3 illustrates the concept of measuring the voltage drop vs. junction temperature relationship for a diode junction. The device under test (DUT) is embedded in hot fluid to heat DUT up to desired temperatures.

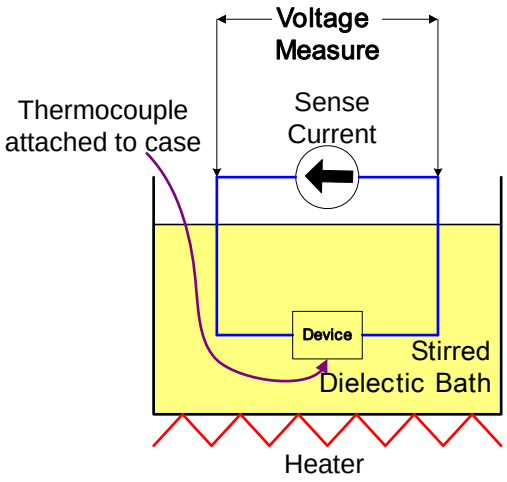



***Figure 9.3 Illustration of the bath method for TSP measurement***

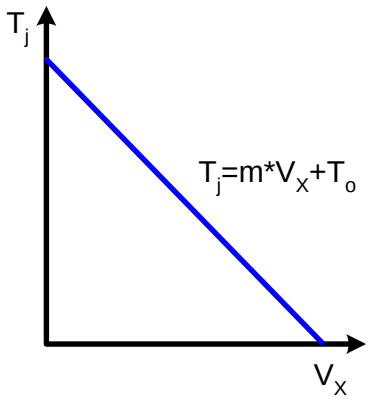



***Figure 9.4 Typical example of a TSP Plot with constant sense current***

When the DUT attains thermal equilibrium with the hot fluid, a sense current is applied to the junction. Then the voltage drop across the junction is measured as a function of the junction temperatures. The amount of sense current should be small enough not to heat the DUT, for instance, 1*mA,* 10*mA* depending on the device type. The measurements are repeated over a specific temperature range with some specified temperature steps. Figure 9.4 shows a typical result.

The relationship between the junction temperature and voltage drop at a given temperature can be expressed as shown in the following equation.

$$T_j = m * V_X + T_o \tag{9.14}$$

The slope, $m(℃/V)$ and the temperature ordinate-intercept, $T_o(V)$ are used to quantify this straight line relationship. The reciprocal of the slope is often referred to as the "K factor $(V/^oC)$". In this case, $V_f(V)$ is the TSP. For semiconductor junctions, the slope *m* of the calibrating straight line in Fig. 9.4 is always negative, i.e., the forward conduction voltage decreases with increasing junction temperature. This process of obtaining equation (9.14) is called the calibration procedure for a given device.

During the thermal resistance measurement test, the junction temperature can be estimated by measuring the voltage drop at a given sense current during the calibration procedure and by using equation (9.14). The TSP varies from device to device, since a specific device does not have the diode voltage TSP. But the transistor saturation voltage can be used in that case. For instance, the gate turn-on voltage can be used as the TSP for an IGBT or a MOSFET.

### *9.2.3 Measurement Procedures*

The thermal resistance test begins by applying a continuous power of known current and voltage to the DUT. The continuous power heats up the DUT to a thermally equilibrated state. While the device is heating, a continuous train of sampling pulses monitors the TSP, i.e., the voltage drop or the same as the junction

temperature. The TSP sampling pulse must provide a sense current equal to that used during the calibration procedure for obtaining equation (9.14). While monitoring the TSP, adjust the applied power so as to insure a sufficient rise in $T_j$. Adjusting the applied power to achieve a $T_j$ increase of about 100℃ above the reference temperature will generate enough temperature difference to ensure a good measurement resolution. A typical example is shown in Fig. 9.5.

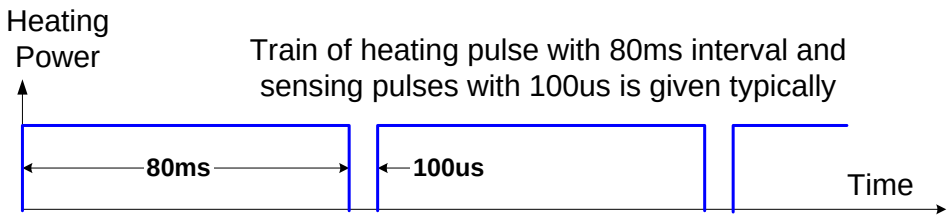
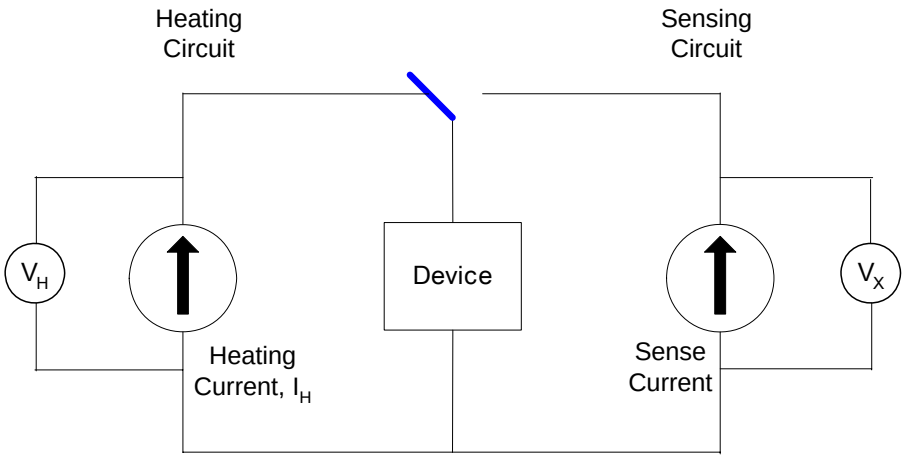



***Figure 9.5 Example of a power and sample pulses train during the $R_{jc}$ measurement of a SPM-IGBT***

The TSP sampling time must be very short so as not to allow for any appreciable cooling of the junction prior to re-applying power. The power and sensing pulse train shown in Fig. 9.5 has a duty cycle of 99.9%, which for all practical purposes is considered to be continuous power. Obviously, most of the total power is applied to the DUT in Fig. 9.6.

Once $T_j$ reaches thermal equilibrium, its value along with the reference temperature $T_c$ and applied power $P$ is recorded. Using the measured values and equation (9.11), the junction-to-case thermal resistance $R_{\theta jc}$ can be estimated. $R_{\theta jc}$ here indicates the ability of a device to dissipate power in an ideal environment, that is, mounted with an infinite or temperature-controlled heat sink.

Figure 9.7 shows the thermal resistance measurement environment for SPMs. The SPM is placed on a heat sink having a large heat carrying capacity. Thermal grease is applied between the SPM and heat sink to prevent an air gap.




$$T_j = m*V_X + T_o$$

$$R_{\theta jc} = (Tj-Tc) / (V_H*I_H)$$

***Figure 9.6 Illustration of the thermal resistance test method concept***

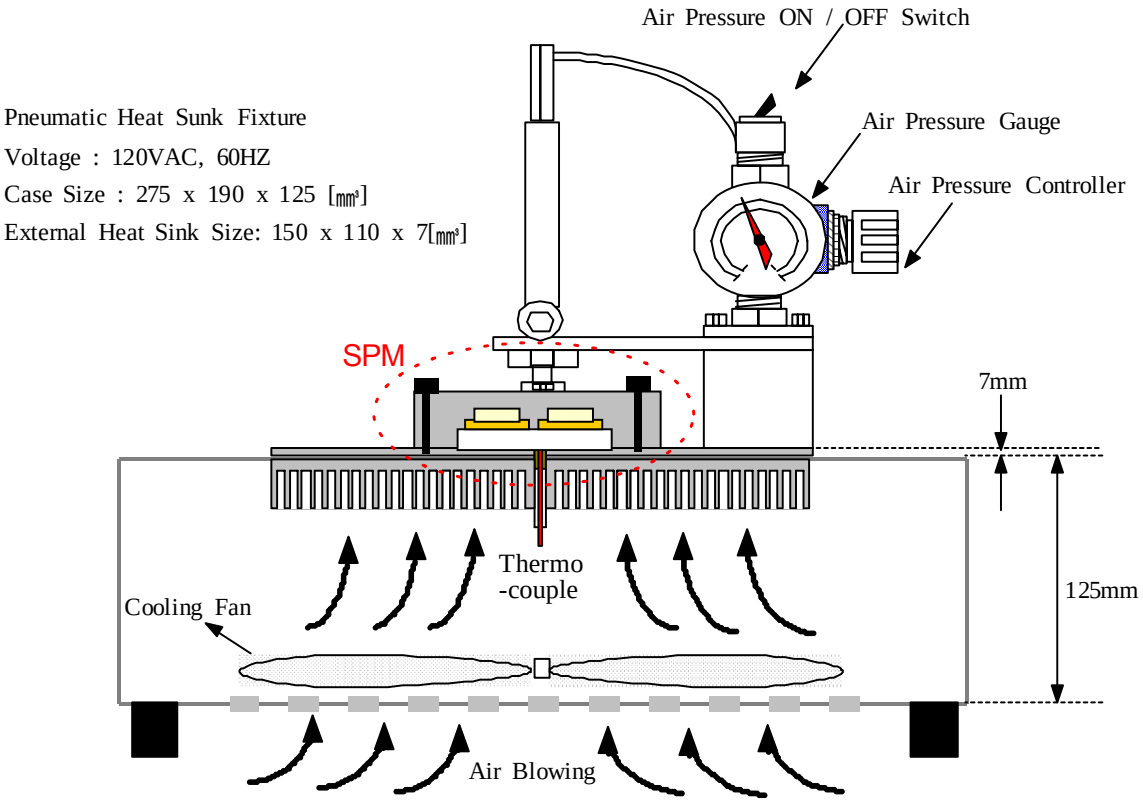



***Figure 9.7 The thermal measurement environment of the SPM.***

A thermocouple is inserted through the heat sink and pressed against the underside of the SPM to

record the SPM surface temperature. Although there is no stipulation on the thermocouple location on which the reference temperature ($T_c$ here) needs to be measured, it is recommended that the ideal location is the hottest point. In this note, the SPM center or the heat sink center was chosen.

The thermocouple needs to make a good thermal contact with its reference location. Thermal grease and appropriate clamping pressure are needed as shown in Fig. 9.7.

## *9.3 Temperature Rise Considerations and Calculation Example*

The result of loss calculation using the typical characteristics is shown in Figure 9.8 as "Effective current versus carrier frequency characteristics". The conditions are follows.

Conditions : $V_{PN}$=300V, $V_{CC}$=$V_{BS}$=15V, $V_{CE(sat)}$=typical, Switching loss=typical, Tj=150°C, Tc=125°C, Rth(j-c) = Max., M.I.=1.0, P.F=0.8, 3-phase continuous PWM modulation, 60Hz sine waveform output.

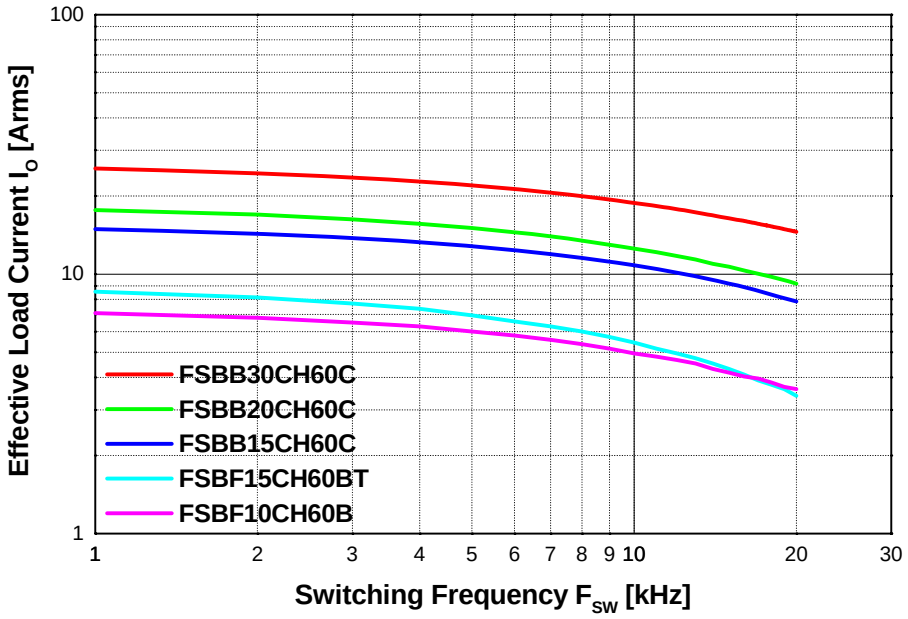



***Figure 9.8 Effective current ─carrier frequency characteristics***

**Note:**

The above characteristics may vary in the different control schemes and motor drive types.

Figure 9.8 indicates an example of an inverter operated under the condition of Tc=125°C. It indicates the effective current Io which can be outputted when the junction temperature Tj rises to the average junction temperature of 150°C (up to which the Mini DIP SPM operates safely).

## *9.4 Heat Sink Design Guide*

The selection of a heat sink is constrained by many factors including set space, actual operating power dissipation, heat sink cost, flow condition around a heat sink, assembly location, etc. In this note, only some of the constraints are analyzed to give some insights in heat sink selection from a practical application point of view.

***Heat Sink for Use in Washing Machines***

The type of heat sink shown in Fig. 9.9 can be applied under natural convection conditions in washing machine applications that have drive characteristics in which the power dissipated is alternatively high and low over periods of hundreds of milli-seconds in the SPM.

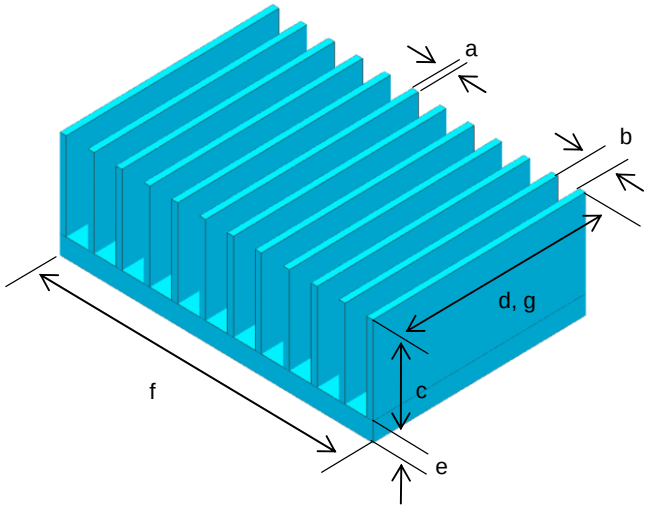



***Figure 9.9 A heat sink example for washing machines applications.***
***a = Fin thickness, b = Fin spacing, c = Fin height, d = Fin length,***
***e = Base-plate thickness, f = Base-plate width, g = Base-plate length***

Figures 9.10 - 9.13 show the analysis results for the heat sink-to-ambient thermal resistance, $R_{\theta ha}$, in designing the heat sink. This varies widely with the changes in fin spacing, fin/base-plate length and fin/base-plate width. It should be noted that the optimum fin spacing is approximately 4 or 5 mm with a base-plate area of 73×53 $mm^2$, as shown in Fig. 9.10. Increasing the fin spacing results in a reduction of the total number of fins, i.e., the total convection area. Reducing the fin spacing interferes with the airflow field between the adjacent fins. This causes an increase in the thermal resistance when the fins are spaced below and above 4mm and 5mm, respectively. An increase in fin thickness decreases the total number of fins and the size of the heat sink, resulting in an increase in thermal resistance.

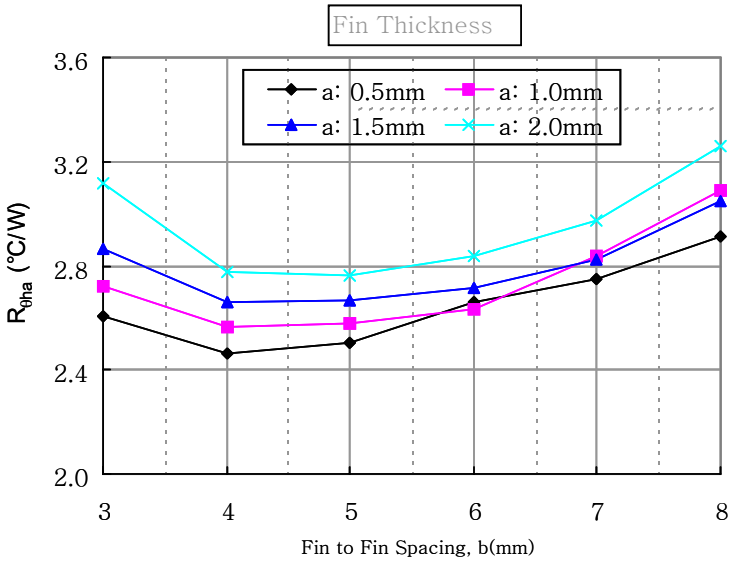



***Figure 9.10 $R_{\theta ha}$ variation by change of the fin spacing.***

***(Constant: c=21mm, d=53mm, e=4mm, f=78mm, g=53mm)***

Figures 9.11 and 9.12 show the results to see the effect of the base-plate length and width on thermal resistance. From Fig. 9.11, we can see that the increase in the length to 150%, that is 79.5mm (53mm×1.5), reduces the resistance to 85% (≅2.3 °C/W), and an increase of 200% (53mm×2=106mm) reduces the resistance to 78% (≅2.09 °C/W). Figure 9.12 is the result of the variation in the base-plate width and it shows that the increase in the width to 150% (78mm×1.5=117mm) and 200% (78mm×2=156mm) reduces the resistance to 79% (≅2.144 °C/W) and 70% (≅1.88 °C/W), respectively. Therefore, increasing the width is more effective reducing the thermal resistance, as compared with increasing the length.

Figure 9.13 shows the thermal resistance variation with a change in the fin height.

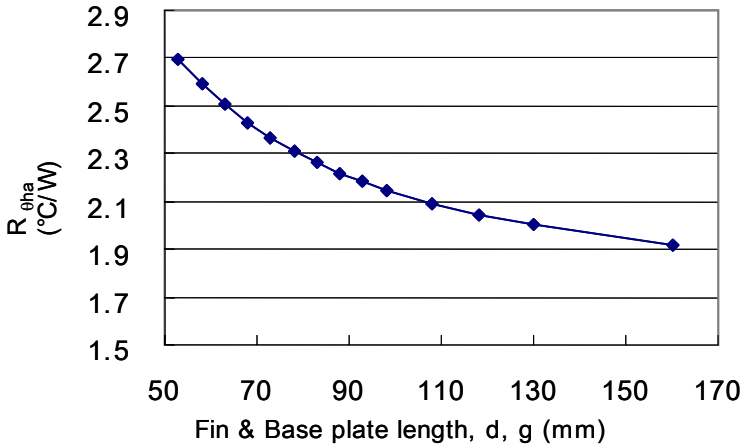



***Figure 9.11 $R_{\theta ha}$ variation by change of the base-plate length.***

***(Content: a=1.5mm, b=5.45mm, c=21mm, e=4mm, f=78mm)***

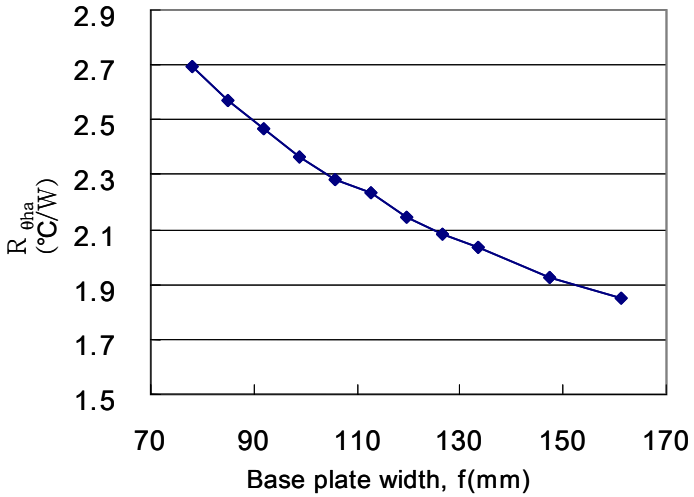



***Figure 9.12 $R_{\theta ha}$ variation by change of the base-plate width.***

***(Constant: a=1.5mm, b=5.45mm, c=21mm, d=53mm, e=4mm, g=53mm)***

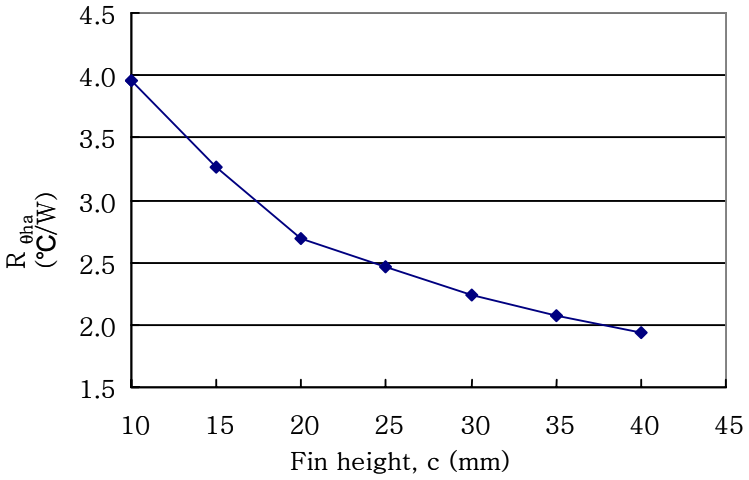



***Figure 9.13 $R_{\theta ha}$ variation by change of the fin height.***

***(Constant: a=1.5mm, b=5.45mm, d=53mm, e=4mm, f=78mm, g=53mm)***

***Heat Sink for Use in Air-Conditioners***

Inverters for air-conditioner applications need continuous power dissipation in the SPM, which are different from those used in washing machines. They generally use a heat sink with forced-convection using a fan for the SPM. Figure 9.14 shows the shape of a heat sink, which is generally used in air conditioning systems. In this section, the airflow velocity effect on the thermal resistance is described based on using the heat sink shown in Fig. 9. 14.

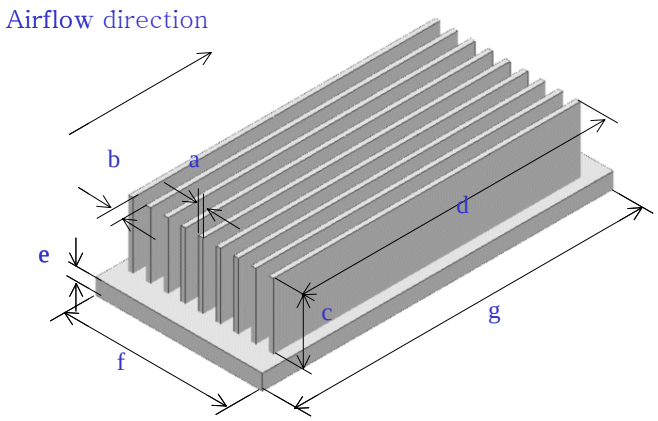



***Figure 9.14 A heat sink example for air-conditioner applications.***

***(Constant: a= 2mm, b= 6mm, c= 30mm, d=140mm, e=7mm, f=76/100mm, g=160mm)***

Figure 9.15 shows the airflow velocity effect on the resistance, $R_{\theta ha}$. Two kinds of heat sink base-plates are used and the reference values of the thermal resistance are around 1.4 °C/W and 1.6 °C/W, respectively, depending on the natural convection condition. We can see that the forced convection reduces the resistance approximately three times. In this case the air velocity is about 2 m/sec, and it is an optimal and cost-effective heat sink size. A fan having a velocity of 5 m/sec., reduces the resistance to 85% (≅0.25 °C/W).

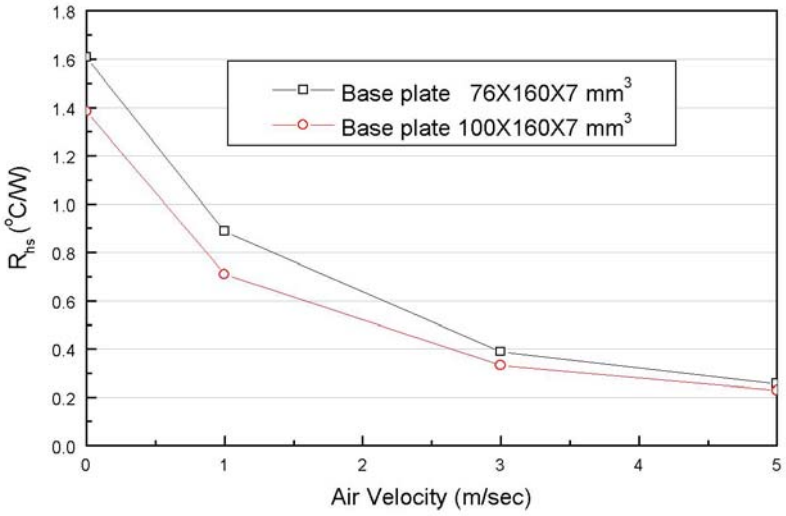



***Figure 9.15 $R_{\theta ha}$ variation by change of airflow velocity.***

# *10. Package*

## *10.1 Heat Sink Mounting*

The following precautions should be observed to maximize the effect of the heat sink and minimize device stress, when mounting an SPM on a heat sink.

***Heat Sink***

Please follow the instructions of the manufacturer, when attaching a heat sink to an Mini DIP SPM. Be careful not to apply excessive force to the device when attaching the heat sink.

Drill holes for screws in the heat sink exactly as specified. Smooth the surface by removing burrs and protrusions of indentations. Refer to Table 10.1.

Heat-sink-equipped devices can become very hot when in operation. Do not touch, as you may sustain a burn injury.

***Silicon Grease***

Apply silicon grease between the SPM and the heat sink to reduce the contact thermal resistance. Be sure to apply the coating thinly and evenly, do not use too much. A uniform layer of silicon grease (100 ~ 200um thickness) should be applied in this situation.

***Screw Tightening Torque***

Do not exceed the specified fastening torque. Over tightening the screws may cause package cracks and bolts and AL heat-fin destruction. Tightening the screws beyond a certain torque can cause saturation of the contact thermal resistance. The tightening torques in table 10.1 is recommended for obtaining the proper contact thermal resistance and avoiding the application of excessive stress to the device.

Avoid stress due to tightening on one side only. Figure 10.1 shows the recommended torque order for mounting screws. Uneven mounting can cause the SPM DBC substrate to be damaged.

***Table 10.1 Torque Rating***

| Item | Condition | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ | Max | |
| Mounting Torque | Mounting Screw : M3 | Recommended 0.62 N·m | 0.51 | 0.62 | 1.00 | N·m |
| DBC Flatness | (Note Fig. 10.1) | | 0 | - | +120 | μm |
| Heatsink Flatness | | | -100 | | +50 | μm |
| Weight | | | - | 15.40 | - | g |

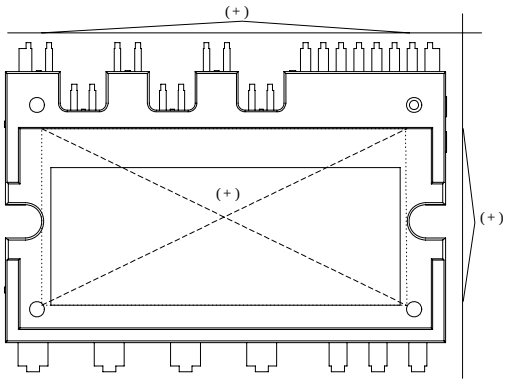



***Figure 10.1 Flatness measurement position***

## *10.2 Handling Precaution*

When using semiconductors, the incidence of thermal and/or mechanical stress to the devices due to improper handling may result in significant deterioration of their electrical characteristics and/or reliability.

***Transportation***

Handle the device and packaging material with care. To avoid damage to the device, do not toss or drop. During transport, ensure that the device is not subjected to mechanical vibration or shock. Avoid getting devices wet. Moisture can also adversely affect the packaging (by nullifying the effect of the antistatic agent). Place the devices in special conductive trays. When handling devices, hold the package and avoid touching the leads, especially the gate terminal. Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause the electrode terminals to be deformed or the resin case to be damaged. Throwing or dropping the packaging boxes might cause the devices to be damaged. Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.

***Storage***

1) Avoid locations where devices will be exposed to moisture or direct sunlight. (Be especially careful during periods of rain or snow.)
2) Do not place the device cartons upside down. Stack the cartons atop one another in an uprighrt position only. : Do not place cartons on their sides.
3) The storage area temperature should be maintained within a range of 5°C to 35°C, with humidity kept within the range from 40% to 75%.
4) Do not store devices in the presence of harmful (especially corrosive) gases, or in dusty conditions.
5) Use storage areas where there is minimal temperature fluctuation. Rapid temperature changes can cause moisture condensation on stored devices, resulting in lead oxidation or corrosion. As a result,

lead solderability will be degraded.

6) When repacking devices, use antistatic containers. Unused devices should be stored no longer than one month.

7) Do not allow external forces or loads to be applied to the devices while they are in storage.

***Environment***

1) When humidity in the working environment decreases, the human body and other insulators can easily become charged with electrostatic electricity due to friction. Maintain the recommended humidity of 40% to 60% in the work environment. Be aware of the risk of moisture absorption by the products after unpacking from moisture-proof packaging.

2) Be sure that all equipment, jigs and tools in the working area are grounded to earth.

3) Place a conductive mat over the floor of the work area, or take other appropriate measures, so that the floor surface is grounded to earth and is protected against electrostatic electricity.

4) Cover the workbench surface with a conductive mat, grounded to earth, to disperse electrostatic electricity on the surface through resistive components. Workbench surfaces must not be constructed of low-resistance metallic material that allows rapid static discharge when a charged device touches it directly.

5) Ensure that work chairs are protected with an antistatic textile cover and are grounded to the floor surface with a grounding chain.

6) Install antistatic mats on storage shelf surfaces.

7) For transport and temporary storage of devices, use containers that are made of antistatic materials of materials that dissipate static electricity.

8) Make sure cart surfaces that come into contact with device packaging are made of materials that will conduct static electricity, and are grounded to the floor surface with a grounding chain.

9) Operators must wear antistatic clothing and conductive shoes (or a leg or heel strap).

10) Operators must wear a wrist strap grounded to earth through a resistor of about 1MΩ.

11) If the tweezers you use are likely to touch the device terminals, use an antistatic type and avoid metallic tweezers. If a charged device touches such a low-resistance tool, a rapid discharge can occur. When using vacuum tweezers, attach a conductive chucking pad at the tip and connect it to a dedicated ground used expressly for antistatic purposes.

12) When storing device-mounted circuit boards, use a board container or bag that is protected against static charge. Keep them separated from each other, and do not stack them directly on top of one another, to prevent static charge/discharge which occurs due to friction.

13) Ensure that articles (such as clip boards) that are brought into static electricity control areas are constructed of antistatic materials as far as possible.

14) In cases where the human body comes into direct contact with a device, be sure to wear finger cots or gloves protected against static electricity.

***Electrical Shock***

A device undergoing electrical measurement poses the danger of electrical shock. Do not touch the device unless you are sure that the power to the measuring instrument is off.

***Circuit Board Coating***

When using devices in equipment requiring high reliability or in extreme environments (where moisture, corrosive gas or dust is present), circuit boards can be coated for protection. However, before doing so, you must carefully examine the possible effects of stress and contamination that may result. There are many and varied types of coating resins whose selection is, in most cases, based on experience. However, because device-mounted circuit boards are used in various ways, factors such as board size, board thickness, and the effects that components have on one another, makes it practically impossible to predict the thermal and mechanical stresses that semiconductor devices will be subjected to.

## *10.3 Marking Specifications*

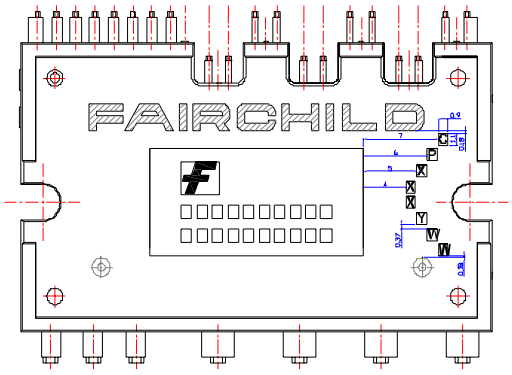



***Figure 10.2 Marking layout (bottom side)***

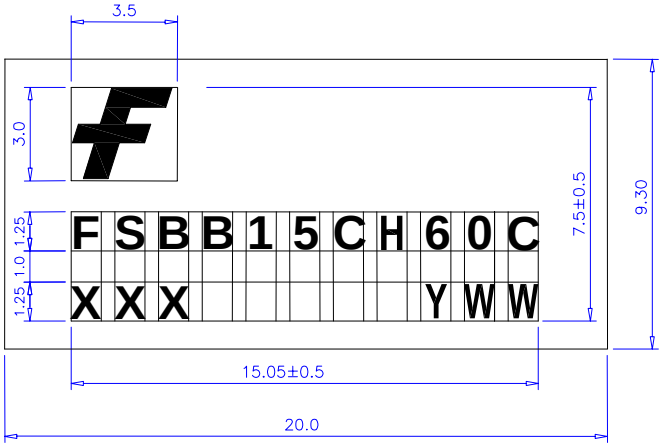


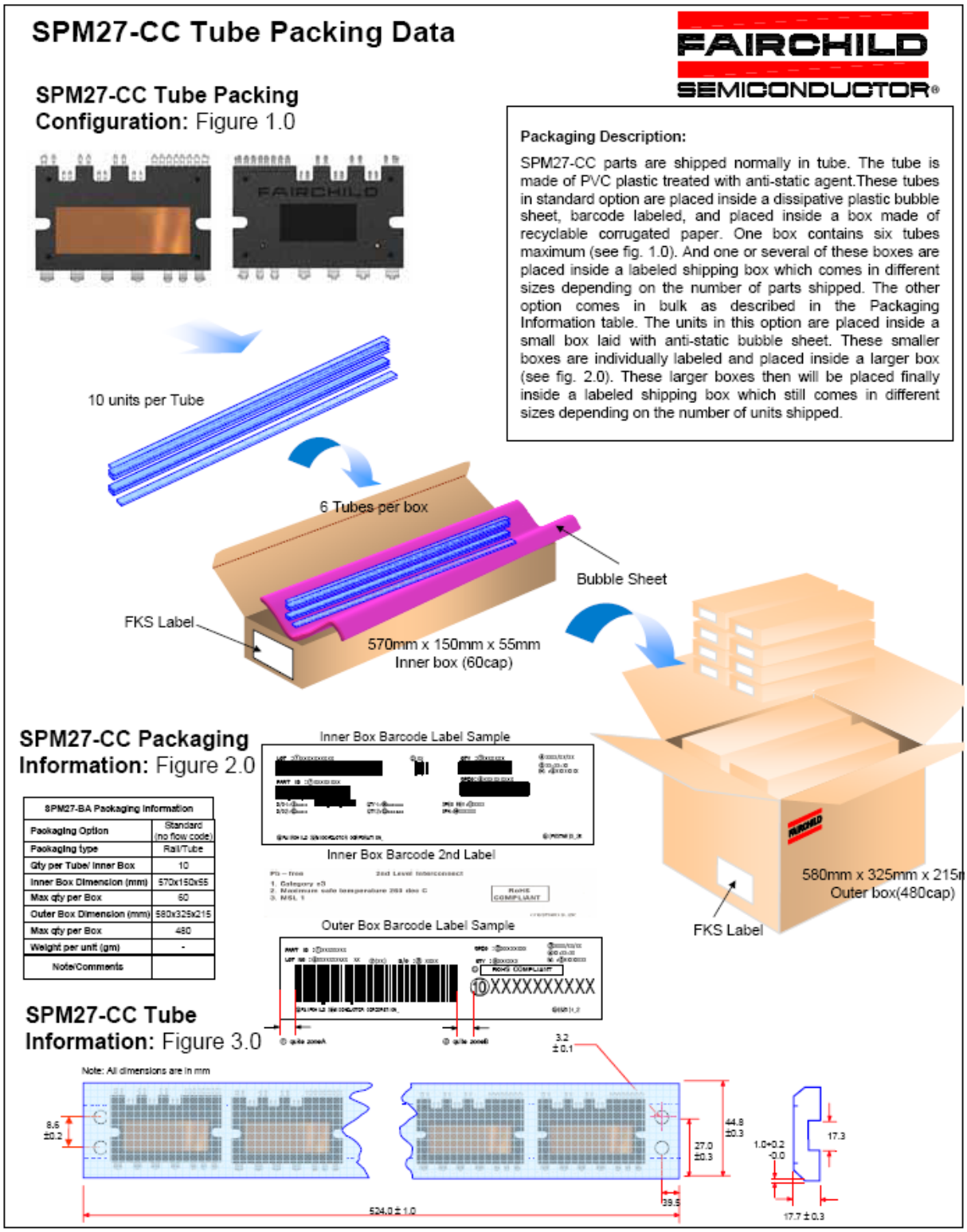

***Figure 10.3 Marking dimension of FSBB15CH60C***

1. F : FAIRCHILD LOGO
2. XXX : Last 3 digits of Lot No.
3. YWW : WORK WEEK CODE ("Y" refers to the below alphabet character table)
4. Hole Side Marking
   - CP : FSBB15CH60C (Product Name)
   - XXX : Last 3 digits of Lot No.
   - YWW : WORK WEEK CODE ("Y" refers to the below alphabet character table)

***Table 10.2 Work Week Code***

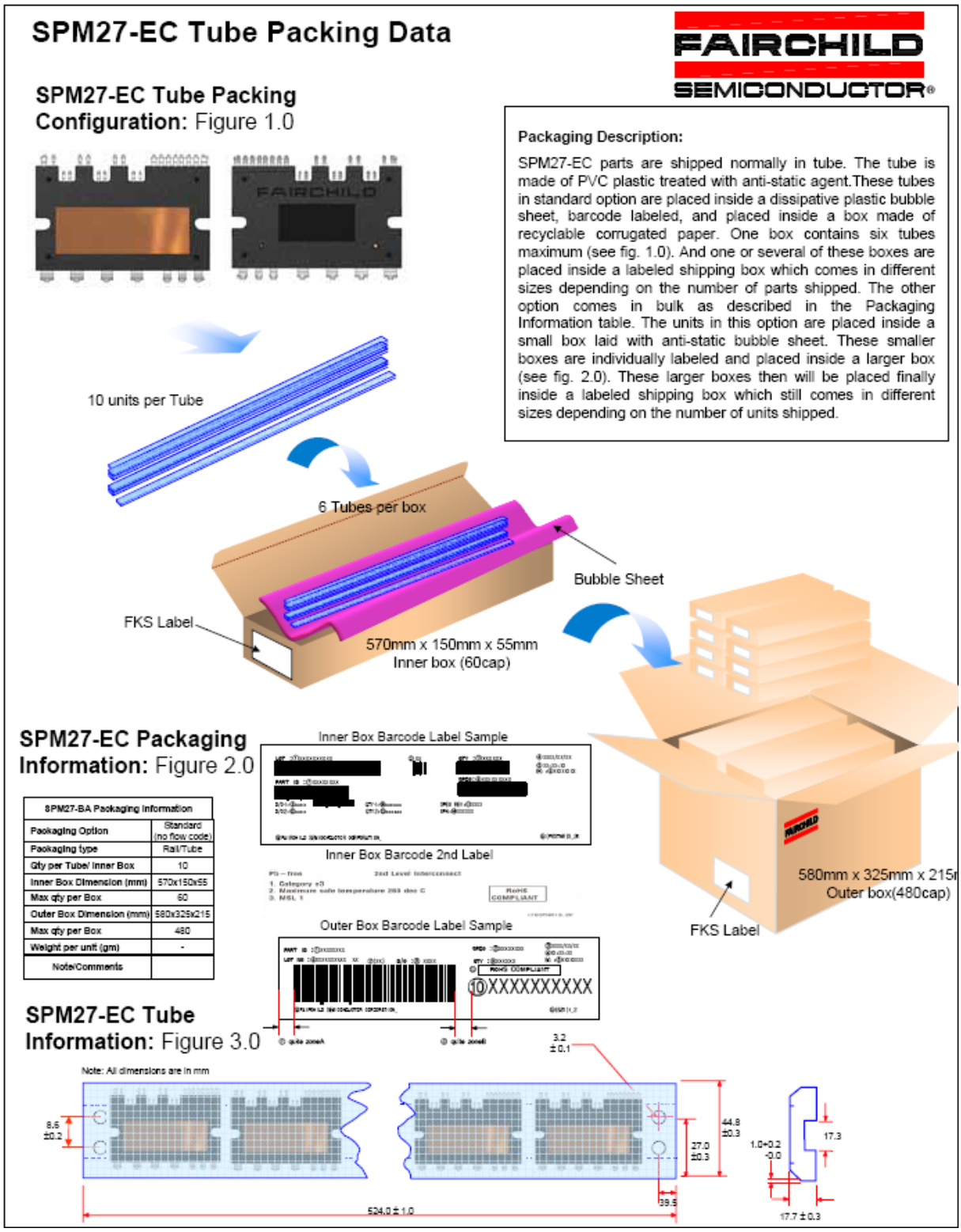
| Y | 2000 | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Alphabet | **A** | **B** | **C** | **D** | **E** | **F** | **G** | **H** | **J** | **K** | **A** |

## *10.4 Packaging Specifications*



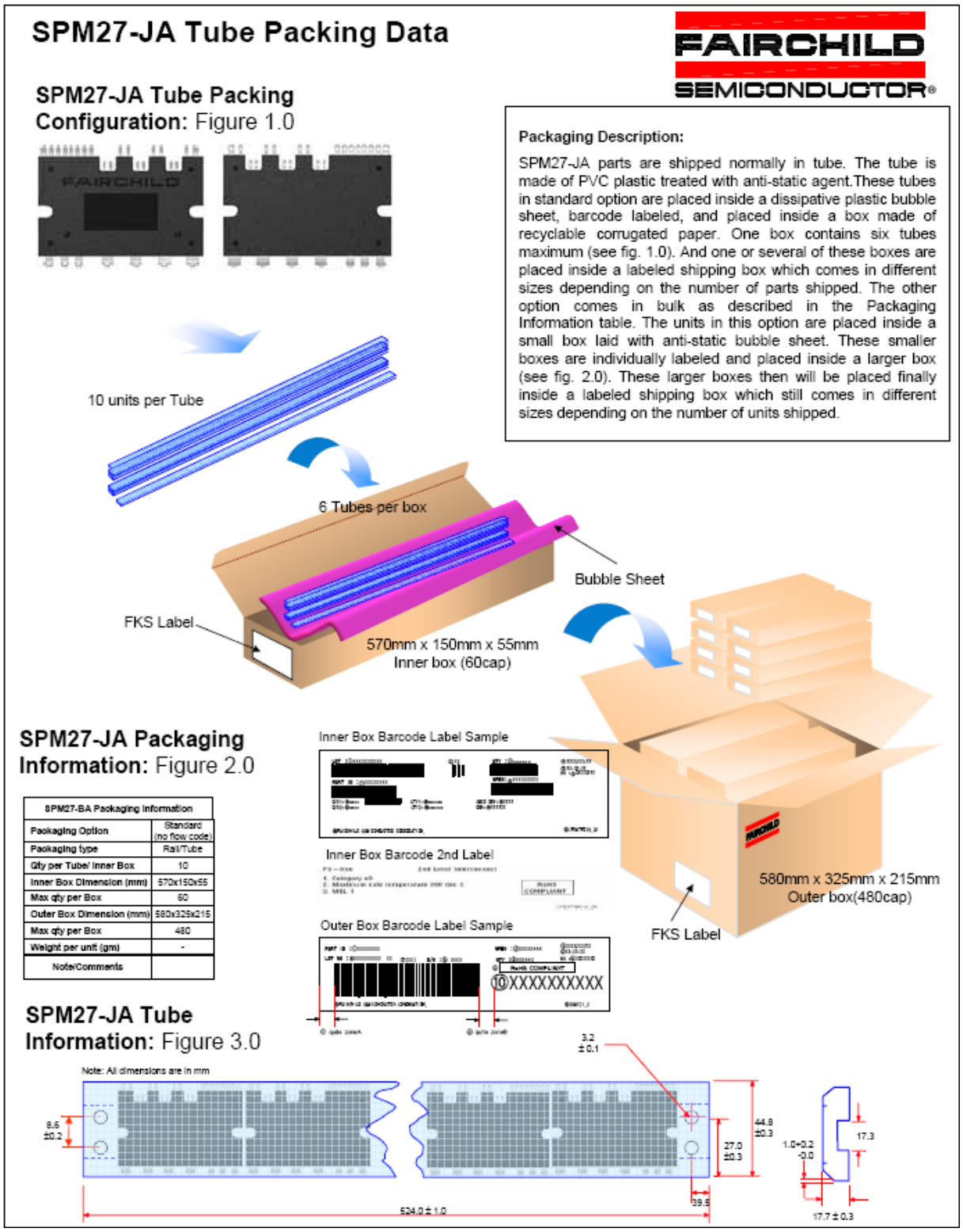

| SPM27-BA Packaging Information | |
|---|---|
| Packaging Option | Standard (no flow code) |
| Packaging type | Rail/Tube |
| Qty per Tube/ Inner Box | 10 |
| Inner Box Dimension (mm) | 570x150x55 |
| Max qty per Box | 60 |
| Outer Box Dimension (mm) | 580x325x215 |
| Max qty per Box | 480 |
| Weight per unit (gm) | - |
| Note/Comments | |

***Figure 10.4 Description of packaging process for SPM27-CC.***




| SPM27-BA Packaging Information | |
|---|---|
| Packaging Option | Standard (no flow code) |
| Packaging type | Rail/Tube |
| Qty per Tube/ Inner Box | 10 |
| Inner Box Dimension (mm) | 570x150x55 |
| Max qty per Box | 60 |
| Outer Box Dimension (mm) | 580x325x215 |
| Max qty per Box | 480 |
| Weight per unit (gm) | - |
| Note/Comments | |

***Figure 10.5 Description of packaging process for SPM27-CC.***




| SPM27-BA Packaging Information | |
|---|---|
| Packaging Option | Standard (no flow code) |
| Packaging type | Rail/Tube |
| Qty per Tube/ Inner Box | 10 |
| Inner Box Dimension (mm) | 570x150x55 |
| Max qty per Box | 60 |
| Outer Box Dimension (mm) | 580x325x215 |
| Max qty per Box | 480 |
| Weight per unit (gm) | - |
| Note/Comments | |

***Figure 10.6 Description of packaging process for SPM27-JA.***

**Notice for Safe Designs**

We are making every effort to improve the quality and reliability of our products. However, there are possibilities that semiconductor products be damaged or malfunctioned. Pay much attention to take safety into consideration and to adopt redundant, fireproof and malfunction-proof designs, so that the breakdown or malfunction of these products would not cause accidents including human life, fire, and social damages.

**Notes When Using this Specification**

This specification is intended as reference materials when customers use Fairchild semiconductor products. Thus, we disclaim any warranty for exercise or our intellectual property rights and other proprietary rights regarding the product information described in this specification.

We assume absolutely no liability in the event of any damage and any infringement of third party's rights arising from the use of product data, diagrams, tables, and application circuit examples described in this specification.

All data including product data, diagrams, and tables described in this specification are correct as of the day it was issued, and they are subject to change without notice. Always verify the latest information of these products with Fairchild semiconductor and its agents before purchase.

The products listed in this specification are not designed to be used with devices or systems, with would directly endanger human life. Should you intend to use these products for special purposes such as transportation equipment, medical instruments, aerospace machinery, nuclear-reactor controllers, fuel controllers, or submarine repeaters, please contact Fairchild semiconductor and its agents.

Regarding transmission or reproduction of this specification, prior written approval of Fairchild semiconductor is required.

Please contact Fairchild semiconductor and its agents if you have any questions about this specification.